Rec'd PCT/PTO 08 MAR 2002

FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER **220167US2PCT**
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 10/069962
INTERNATIONAL APPLICATION NO **PCT/JP00/04602**	INTERNATIONAL FILING DATE **10 July 2000**	PRIORITY DATE CLAIMED **none**

TITLE OF INVENTION
EVEN HARMONIC MIXER

APPLICANT(S) FOR DO/EO/US
SHIMOZAWA Mitsuhiro et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   - a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   - b. ☒ has been communicated by the International Bureau.
   - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   - a. ☒ is attached hereto.
   - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   - a. ☐ are attached hereto (required only if not communicated by the International Bureau)
   - b. ☐ have been communicated by the International Bureau.
   - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

    PCT/IB/308
    Form PTO-1449
    Drawings (18 sheets)
    Cited References (2)

PCTUS1/REV03

10/069962 JC19 Rec'd PCT/PTO 08 MAR 2002

U.S. APPLICATION NO (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
10/069962	PCT/JP00/04602	220167US2PCT

24. The following fees are submitted..

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS	PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$1040.00**		
☒ International preliminary examination fee (37 CFR 1 482) not paid to USPTO but International Search Report prepared by the EPO or JPO	**$890.00**		
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$740.00**		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$710.00**		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =		**$890.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	8 - 20 =	0	x $18.00	**$0.00**	
Independent claims	1 - 3 =	0	x $84.00	**$0.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$890.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$890.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1 492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$890.00**	
Fee for recording the enclosed assignment (37 CFR 1 21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
TOTAL FEES ENCLOSED =				**$890.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$890.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No ________ in the amount of ________ to cover the above fees. A duplicate copy of this sheet is enclosed

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

22850

Surinder Sachar
Registration No. 34,423

Surinder Sachar
SIGNATURE

Marvin J. Spivak
NAME

24,913
REGISTRATION NUMBER

March 8 2002
DATE

181PRTS 10/069962

JC19 Rec'd PCT/PTO 08 MAR 2002

SPECIFICATION

Title of the Invention

Even harmonic mixer

Field of the Invention

The present invention relates to an even harmonic mixer for use in transmitter-receivers intended for a radio communications system. More particularly, it relates to an even harmonic mixer that not only converts the frequency of a high frequency signal but also is suitable for a quadrature modulator and a quadrature demodulator for use with a modulation method, such as GMSK, QPSK, or QAM, which is frequently used in a digital radio communication system.

Background of the Invention

There is an even harmonic mixer which employs an antiparallel diode pair (APDP) as a means of mixing high-frequency signals. The principle of such an even harmonic mixer has been described in "Harmonic mixing with an antiparallel diode pair" by Marvin Cohn and et al., IEEE Transactions on Microwave theory and techniques, Vol. MTT-23, No. 8, pp. 667 to 673, August 1975. Fig. 1 is a schematic circuit diagram showing the structure of the prior art even harmonic mixer described in this reference. In the figure, reference numerals 1a and 1b denote first and second diodes, and reference numeral 2 denotes an APDP that consists of these diodes 1a and 1b. As shown in Fig. 1, in the APDP 2, the first and second diodes 1a and 1b are connected in parallel to each other so that they are opposite in polarity. Reference numeral 3 denotes a

demultiplexing circuit, reference numeral 4 denotes a high-pass filter (HPF) included in the demultiplexing circuit 3 and having an end connected to an RF terminal 7, reference numeral 5 is band-pass filter (BPF) included in the demultiplexing circuit 3 and having an end connected to another end of the HPF 4 and the APDP 2, and another end connected to an LO terminal 8, and reference numeral 6 denotes a low-pass filter (LPF) included in the demultiplexing circuit 3 and having an end connected to the HPF 4, the BPF 5, and the APDP 2, and another end connected to an IF terminal 9.

Next, a description will be made as to the operation of the prior art even harmonic mixer.

When the even harmonic mixer shown in Fig. 1 operates as a mixer for reception, a high frequency signal (RF signal) and a local oscillation wave (LO wave) are applied to the demultiplexing circuit 3 by way of the RF terminal 7 and the LO terminal 8, respectively. The RF signal applied to the RF terminal 7 is input to the APDP 2 by way of the HPF 4 of the demultiplexing circuit 3. At this time, leakage of the RF signal to the LO terminal 8 is prevented by the BPF 5. Furthermore, the LO wave applied to the LO terminal 8 is input to the APDP 2 by way of the BPF 5. At this time, leakage of the LO wave to the RF terminal 7 is prevented by the HPF 4. An intermediate-frequency signal (IF signal) is generated from the RF signal and the LO wave applied to the APDP 2. The generated IF signal is output to the IF terminal 9 which is an output signal terminal by way of the LPF 6. At this time, the RF signal and the LO wave are blocked by the LPF 6.

When the even harmonic mixer shown in Fig. 1 operates as a mixer for transmission, an IF signal and an LO wave are applied

to the demultiplexing circuit 3 by way of the IF terminal 9 and the LO terminal 8, respectively. The IF signal applied to the IF terminal 9 is input to the APDP 2 by way of the LPF 6. At this time, leakage of the IF signal to the RF terminal 7 is prevented by the HPF 4. Furthermore, leakage of the IF signal to the LO terminal 8 is prevented by the BPF 5. In addition, the LO wave applied to the LO terminal 8 is input to the APDP 2 by way of the BPF 5. At this time, leakage of the LO wave to the RF terminal 7 is prevented by the HPF 4. The APDP 2 generates an RF signal from the IF signal and the LO wave applied thereto. The generated RF signal is output to the RF terminal 7 which is an output signal terminal by way of the HPF 4.

Next, a frequency conversion operation will be explained.

Fig. 2 shows a relationship between a voltage across the APDP 2 and an electric current flowing through the APDP 2 which constitutes the even harmonic mixer. Since the first and second diodes 1a and 1b are connected in parallel to each other so that they are opposite in polarity, an electric current flows through the first diode 1a when the applied voltage is negative, whereas an electric current flows through the second diode 1b when the applied voltage is positive. By the way, the electric current which flows through each diode is generally given by the following equation.

$$I = Is*(\exp(qV/kT)-1) \qquad (1)$$

where Is is a saturation current, q is an electric charge, V is the applied voltage, k is Boltzmann's constant, and T is absolute temperature. When the electric current given by equation (1) shows a characteristic that it hardly flows until

the applied voltage V reaches a certain value Vt, and rapidly increases when the applied voltage V exceeds Vt. Therefore, the APDP 2 which consists of the first and second diodes 1a and 1b can be assumed to be an element which has a DC characteristic that the electric current flows only when the following condition: V>Vt or V<-Vt is established, as shown in Fig. 2. When applying an LO wave having an amplitude of Vp shown in Fig. 3 to the APDP 2 having such a DC characteristic, no electric current flows through either of the two diodes when the LO wave amplitude is in the range of -Vt from +Vt, and either one of the two diodes is turned on and an electric current therefore flows through the one of them when the LO wave amplitude exceeds +Vt or is less than -Vt, as shown in Fig. 4. As a result, the APDP 2 operates in such a manner that a low-frequency electric current whose phase changes in a half cycle thereof flows through the APDP 2, as shown in Fig. 5(a), and its conductance g given by the following equation increases in a half cycle of the electric current, as shown in Fig. 5(b).

$$g = dI/dV \qquad (2)$$

Fig. 5(b) means that the conductance g changes at a frequency two times that of the LO wave. Actually, when the waveform of the conductance is Fourier-analyzed, the term having a period twice that of the LO wave has a large coefficient. Thus, the even harmonic mixer, which employs the APDP 2, can output a mixture wave of the second harmonic of the LO wave and the input signal.

The prior art even harmonic mixer shown in Fig. 1 can operate with an LO wave of a frequency that is one-half of a desired frequency of an RF signal. Therefore, the even harmonic mixer

is applied to a transceiver for microwaves, especially, for millimeter waves, as disclosed in most public references including the above-mentioned reference. Since the even harmonic mixer can thus reduce the frequency of the LO wave to the half, transceivers that contains such an even harmonic mixer are expected to drop in price.

However, a problem with the even harmonic mixer which employs such an APDP is that the conversion gain, which is the ratio of the output signal to the input signal, changes greatly with a change in the LO wave electric power structurally. Fig. 6(a) is a graph showing an electric current which flows through the APDP 2 when the amplitude of an LO wave applied to the APDP is set to be equal to or less than its optimum value, Fig. 6(b) is a graph showing an electric current which flows through the APDP 2 when the amplitude of the LO wave applied to the APDP is set to be equal to its optimum value, and Fig. 6(c) is a graph showing an electric current which flows through the APDP 2 when the amplitude of the LO wave applied to the APDP is set to be equal to or greater than its optimum value. When the amplitude of the LO wave is set to be equal to or less than its optimum value, as shown in Fig. 6(a), an adequate conductance is not acquired and the conversion gain therefore decreases remarkably because the LO wave amplitude is insufficient. When the LO wave having an optimum amplitude is applied to the APDP 2, as shown in Fig. 6(b), an adequate conversion gain is acquired. When the LO wave having an amplitude equal to or greater than its optimum value is applied to the APDP 2, as shown in Fig. 6(c), the waveform of the electric current which flows through the APDP 2 becomes a sine wave having the same period as the LO wave. Therefore, in the Fourier series of the conductance, the term

with a period that is twice that of the LO wave has a small coefficient, and the level of a desired mixture wave which is a mixture of the second harmonic of the LO wave and the input signal decreases and the conversion gain therefore decreases. Fig. 7 shows such dependence of the conversion gain on the LO wave electric power. As can be seen from the figure, the conversion gain reaches its maximum value at a certain LO wave electric power and the conversion gain decreases before and behind the certain LO wave electric power.

Furthermore, since the saturation current Is in the above-mentioned equation (1) is a function of absolute temperature T and T is included in the exponential function of the equation (1), the DC characteristic of each diode has temperature dependence. Fig. 8 is a graph showing the temperature dependence of the DC characteristic of the APDP 2 equipped with the two diodes which have such temperature dependence and which are connected in parallel so that they are opposite in polarity. The threshold voltage Vt at which the electric current begins to flow through the APDP decreases with an increase in the temperature of each diode of the APDP. In other words, the threshold voltage becomes lower at a high temperature, whereas the threshold voltage becomes higher at a low temperature. Therefore, the dependence of the conversion gain on the LO wave electric power differs depending on the temperature of each diode of the APDP, as shown in Fig. 9. Therefore, even at the same electric power of the LO wave, the conversion gain differs according to the temperature of each diode of the APDP.

A problem with a prior art even harmonic mixer constructed as mentioned above is that the dependence of the conversion gain

on the LO wave electric power and the temperature dependence of the conversion gain must be considered when designing a communication apparatus and additional cost is therefore required. Another problem is that the level of the LO wave electric power supplied to the even harmonic mixer changes with variations in part performance, and variations in the characteristics of the even harmonic mixer and variations in part performance conspire to make the conversion gain of the prior art even harmonic mixer change greatly. A further problem is that at low temperatures since the conversion gain decreases the noise figure is deteriorated and the receiver sensitivity therefore decreases in receivers, and a desired output is not acquired in transmitters, whereas at high temperatures the conversion gain rises, the signal level rises, and distortion occurs at a stage located behind the even harmonic mixer.

The present invention is proposed to solve the above-mentioned problems, and it is therefore an object of the present invention to provide an even harmonic mixer capable of reducing the amount of change in the conversion gain resulting from a change in the amplitude of an LO wave applied thereto and a change in the temperature of each diode of an APDP included in the even harmonic mixer.

Disclosure of the Invention

An even harmonic mixer in accordance with an aspect of the present invention comprises an antiparallel diode pair means including a first series unit in which a first diode and a first resistor are connected in series and a second series unit in which a second diode and a second resistor are connected in series, the first and second series units being connected in parallel

so that the first and second diodes are opposite in polarity.

Accordingly, the aspect of the present invention offers an advantage of being able to reduce the amount of change in the conversion gain resulting from a change in the LO wave electric power and a change in the temperature of each diode of the antiparallel diode pair means because an electric current, which flows through each diode of the antiparallel diode pair means, can be kept nearly constant regardless of the amplitude of an LO wave applied to the antiparallel diode pair means and the temperature of each diode.

In the even harmonic mixer in accordance with another aspect of the present invention, the first series unit has a plurality of diodes in series which are connected in series to the first resistor, and the second series unit has a plurality of diodes in series which are connected in series to the second resistor.

Accordingly, the other aspect of the present invention offers an advantage of being able to provide an excellent distortion characteristic.

In the even harmonic mixer in accordance with a further aspect of the present invention, the first series unit has a first capacitor connected in parallel to the first resistor and the second series unit has a second capacitor connected in parallel to the second resistor.

Accordingly, the further aspect of the present invention offers an advantage of preventing a decrease in the level of an RF signal applied to the antiparallel diode pair means caused by the resistor connected in series to each diode because the RF signal passes through either the first capacitor or the second capacitor without passing through either the first resistor or

the second resistor.

In the even harmonic mixer in accordance with another aspect of the present invention, the first resistor is connected to a cathode of the first diode in the first series unit and the second resistor is connected to an anode of the second diode in the second series unit so that the first and second resistors are connected to each other at an end of the antiparallel diode pair means. The even harmonic mixer further comprises a first capacitor having an end connected to a node between the first resistor and the first diode and a second capacitor having an end connected to a node between the second resistor and the second diode, an IF signal is input and output by way of a node between the first and second resistors, other ends of the first and second capacitors are connected to each other, an LO wave is applied to a node between the other ends of the first and second capacitors, and an RF signal is input and output by way of the node between the other ends of the first and second capacitors.

Accordingly, the other aspect of the present invention offers an advantage of being able to reduce the amount of change in the conversion gain of the even harmonic mixer resulting from a change of the LO wave electric power and a change in the temperature of each diode of the antiparallel diode pair means, and to prevent a decrease in the level of an RF signal applied to the antiparallel diode pair means caused by the resistor connected in series to each diode.

In the even harmonic mixer in accordance with a further aspect of the present invention, the first resistor is connected to a cathode of the first diode in the first series unit and the second resistor is connected to an anode of the second diode in the second series unit so that the first and second resistors

are connected to each other at an end of the antiparallel diode pair means. The first series unit has a first capacitor connected in parallel to the first resistor and the second series unit has a second capacitor connected in parallel to the second resistor. The even harmonic mixer further comprises a third capacitor having an end connected to a node between the first resistor and the first diode and a fourth capacitor having an end connected to a node between the second resistor and the second diode, an IF signal is input and output by way of a node between the first and second resistors, other ends of the third and fourth capacitors are connected to each other, an LO wave is applied to a node between the other ends of the third and fourth capacitors, and an RF signal is input and output by way of the node between the other ends of the third and fourth capacitors.

Accordingly, the further aspect of the present invention offers an advantage of being able to reduce the amount of change in the conversion gain of the even harmonic mixer resulting from a change of the LO wave electric power and a change in the temperature of each diode of the antiparallel diode pair means, and to prevent a decrease in the level of an RF signal applied to the antiparallel diode pair means caused by the resistor connected in series to each diode.

In the even harmonic mixer in accordance with another aspect of the present invention, the first resistor is connected to a cathode of the first diode in the first series unit and the second resistor is connected to an anode of the second diode in the second series unit so that the first and second resistors are connected to each other at an end of the antiparallel diode pair means, and the first series unit comprises a first capacitor connected to an anode of the first diode and the second series

unit comprises a second capacitor connected to a cathode of the second diode. The even harmonic mixer further comprises a third resistor having an end connected to the anode of the first diode, a fourth resistor having an end connected to the cathode of the second diode and another end connected to another end of the third resistor, a third capacitor having an end connected to a node between the first resistor and the first diode, and a fourth capacitor having an end connected to a node between the second resistor and the second diode, an IF signal is input and output by way of a node between the first and second resistors, other ends of the third and fourth capacitors are connected to each other, an LO wave is applied to a node between the other ends of the third and fourth capacitors, and an RF signal is input and output by way of the node between the other ends of the third and fourth capacitors.

Accordingly, the other aspect of the present invention offers an advantage of being able to reduce the amount of change in the conversion gain of the even harmonic mixer resulting from a change of the LO wave electric power and a change in the temperature of each diode of the antiparallel diode pair means, and to prevent a decrease in the level of an RF signal applied to the antiparallel diode pair means caused by the resistor connected in series to each diode.

In the even harmonic mixer in accordance with a further aspect of the present invention, the first resistor is connected to a cathode of the first diode in the first series unit and the second resistor is connected to an anode of the second diode in the second series unit so that the first and second resistors are connected to each other at an end of the antiparallel diode pair means, and the first series unit comprises a third resistor

connected in series to an anode of the first diode and a first capacitor connected in parallel to the third resistor and the second series unit comprises a fourth resistor connected in series to a cathode of the second diode and a second capacitor connected in parallel to the fourth resistor. The even harmonic mixer further comprises a third capacitor having an end connected to a node between the first resistor and the first diode and a fourth capacitor having an end connected to a node between the second resistor and the second diode, an IF signal is input and output by way of a node between the first and second resistors, other ends of the third and fourth capacitors are connected to each other, an LO wave is applied to a node between the other ends of the third and fourth capacitors, and an RF signal is input and output by way of the node between the other ends of the third and fourth capacitors.

Accordingly, the further aspect of the present invention offers an advantage of being able to reduce the amount of change in the conversion gain of the even harmonic mixer resulting from a change of the LO wave electric power and a change in the temperature of each diode of the antiparallel diode pair means, and to prevent a decrease in the level of an RF signal applied to the antiparallel diode pair means caused by the resistor connected in series to each diode.

In the even harmonic mixer in accordance with another aspect of the present invention, the first resistor is connected to a cathode of the first diode in the first series unit and the second resistor is connected to an anode of the second diode in the second series unit so that the first and second resistors are connected to each other at an end of the antiparallel diode pair means, and the first series unit comprises a first capacitor

connected in parallel to the first resistor and a third capacitor connected in series to an anode of the first diode and the second series unit comprises a second capacitor connected in parallel to the second resistor and a fourth capacitor connected in series to a cathode of the second diode. The even harmonic mixer further comprises a third resistor having an end connected to the anode of the first diode and a fourth resistor having an end connected to the cathode of the second diode and another end connected to another end of the third resistor.

Accordingly, the other aspect of the present invention offers an advantage of being able to reduce the amount of change in the conversion gain of the even harmonic mixer resulting from a change of the LO wave electric power and a change in the temperature of each diode of the antiparallel diode pair means, and to prevent a decrease in the level of an RF signal applied to the antiparallel diode pair means caused by the resistor connected in series to each diode.

Brief Description of the Figures

Fig. 1 is a schematic circuit diagram showing the structure of a prior art even harmonic mixer;

Fig. 2 is a graph showing a DC characteristic of an APDP for use in the prior art even harmonic mixer;

Fig. 3 is a diagram showing the waveform of an LO wave applied to the APDP;

Fig. 4 is a graph showing a relationship between the waveform of the LO wave applied to the APDP and the waveform of a current which flows through the APDP;

Figs. 5(a) and 5(b) are graphs showing the waveform of a current which flows through each diode of the APDP and a

time-varying conductance of each diode;

Fig. 6(a), 6(b), and 6(c) are graphs showing the waveform of the current which flows through the APDP when setting the amplitude of the LO wave applied to the APDP to less than an optimum value, when setting it to the optimum value, and when setting it to greater than the optimum value;

Fig. 7 is a graph showing the dependence of a conversion gain of the prior art even harmonic mixer on the power of the LO wave;

Fig. 8 is a graph showing the temperature dependence of the DC characteristic of the APDP for use in the prior art even harmonic mixer;

Fig. 9 is a graph showing a change in the dependence of the conversion gain of the prior art even harmonic mixer on the LO wave power according to changes in temperature;

Fig. 10 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a first embodiment of the present invention;

Fig. 11 is a graph showing a DC characteristic of an APDP for use in the even harmonic mixer according to the first embodiment of the present invention;

Fig. 12 is a graph showing the dependence of the conversion gain of the even harmonic mixer according to the first embodiment of the present invention on the power of an LO wave applied to the even harmonic mixer;

Fig. 13 is a graph showing the temperature dependence of the DC characteristic of the APDP for use in the even harmonic mixer according to the first embodiment of the present invention;

Fig. 14 is a graph showing a change in the dependence of the conversion gain of the even harmonic mixer according to

the first embodiment of the present invention on the LO wave power according to changes in temperature;

Fig. 15 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the first embodiment of the present invention;

Fig. 16 is a schematic circuit diagram showing the structure of an even harmonic mixer according to another variant of the first embodiment of the present invention;

Fig. 17 is a schematic circuit diagram showing the structure of another example of the APDP for use in the even harmonic mixer according to the first embodiment of the present invention;

Fig. 18 is a schematic circuit diagram showing the structure of another example of the APDP for use in the even harmonic mixer according to the first embodiment of the present invention;

Fig. 19 is a schematic circuit diagram showing the structure of another example of the APDP for use in the even harmonic mixer according to the first embodiment of the present invention;

Fig. 20 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a second embodiment of the present invention;

Fig. 21 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a third embodiment of the present invention;

Fig. 22 is a diagram showing a flow of an RF signal in an APDP for use in the even harmonic mixer according to the third embodiment of the present invention;

Fig. 23 is a schematic circuit diagram showing the

structure of an even harmonic mixer according to a variant of the third embodiment of the present invention;

Fig. 24 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a fourth embodiment of the present invention;

Fig. 25 is a diagram showing a flow of an RF signal in an APDP for use in the even harmonic mixer according to the fourth embodiment of the present invention;

Fig. 26 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the fourth embodiment of the present invention;

Fig. 27 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a fifth embodiment of the present invention;

Fig. 28 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the fifth embodiment of the present invention;

Fig. 29 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a sixth embodiment of the present invention;

Fig. 30 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the sixth embodiment of the present invention;

Fig. 31 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a seventh embodiment of the present invention;

Fig. 32 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the seventh embodiment of the present invention;

Fig. 33 is a schematic circuit diagram showing the

structure of an even harmonic mixer according to an eighth embodiment of the present invention; and

Fig. 34 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the eighth embodiment of the present invention.

Preferred Embodiments of the Invention

Hereafter, to explain the present invention more in detail, the preferred embodiments which embody the present invention will be explained with reference to the accompanied drawings.

Embodiment 1.

Fig. 10 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a first embodiment of the present invention. In the figure, reference numerals 1a and 1b denote first and second diodes, respectively, reference numerals 10a and 10b denote first and second resistors, respectively, and reference numeral 11 denotes an antiparallel diode pair unit (antiparallel diode pair means) that consists of the first and second diodes 1a and 1b and the first and second resistors 10a and 10b. In the following, the antiparallel diode pair unit is abbreviated as APDP. As shown in Fig. 10, in the APDP 11, the first and second diodes 1a and 1b are connected in parallel so that they are opposite in polarity and the corresponding resistor is connected in series to the cathode of each of those diodes. In other words, the APDP 11 consists of a first series unit in which the first diode 1a and the first resistor 10a are connected in series and a second series unit in which the second diode 1b and the second resistor 10b are connected in series, the first and second series units being connected in parallel so that the first and second diodes 1a

and 1b are opposite in polarity.

Furthermore, reference numeral 3 denotes a demultiplexing circuit, reference numeral 4 denotes a HPF included in the demultiplexing circuit 3 and having an end connected to an RF terminal 7, reference numeral 5 denotes a BPF included in the demultiplexing circuit 3 and having an end connected to both another end of the HPF 4 and an end of the APDP 11, and another end connected to an LO terminal 8, reference numeral 6 denotes a LPF included in the demultiplexing circuit 3 and having an end connected to the other end of the HPF 4, the end of the BPF 5, and the end of the APDP 11, and another end connected to an IF terminal 9. The other end of the APDP 11 is connected to a ground potential.

Next, a description will be made as to the operation of the even harmonic mixer according to the first embodiment.

Fig. 11 is a graph showing a relationship between a voltage across the terminals of the APDP 11 and an electric current which flows through the APDP 11 at room temperatures. In the following, the operation of the even harmonic mixer according to the first embodiment will be explained with reference to Fig. 11. Like a prior art APDP, the APDP 11 shows a DC characteristic that the electric current hardly flows until the voltage V applied across its terminals reaches a certain value Vt, and increases rapidly when V exceeds Vt. Therefore, it can be assumed that the APDP 11 according to the first embodiment to be an element having a DC characteristic that the electric current flows only when the following condition: V>Vt or V<-Vt is established, as shown in Fig. 11. However, a rate of increase of the electric current which flows through the APDP 11 according to an increase in the terminal voltage of the APDP 11 is smaller than that of

the prior art APDP 2. The change in the electric current which flows through the APDP 11 is an extremely small even if the terminal voltage changes somewhat. In other words, since the electric current, which flows through each diode of the APDP, can be kept nearly constant regardless of the amplitude of an LO wave applied to the APDP and the temperature of each diode, variations in the conductance can be reduced. Therefore, when an LO wave is applied to the APDP 11 having such a DC characteristic, the amount of change in the conversion gain resulting from a change in the LO wave electric power and a change in the temperature of each diode of the APDP can be reduced.

Fig. 12 is a graph showing a relationship between the electric power of an LO wave applied to the APDP 11 in which the first and second resistors 10a and 10b are connected in series to the first and second diodes 1a and 1b, respectively, as shown in Fig. 10, and the conversion gain. While the conversion gain increases rapidly when the electric power of the LO wave applied to the APDP 11 exceeds a threshold value, as in the case of the DC characteristic shown in Fig. 11, the conversion gain reaches its maximum value when the LO wave electric power reaches a predetermined value Po, and the conversion gain then decreases slowly as the LO wave electric power exceeds Po and increases. Thus, the APDP 11 according to the first embodiment has a dependence of the conversion gain on the LO wave electric power that the amount of change in the conversion gain resulting from a change in the LO wave electric power is small when the LO wave electric power exceeds the predetermined value Po. Therefore, the amount of change in the conversion gain resulting from the change in the LO wave electric power can be reduced.

In addition to the above-mentioned advantage of providing

a small dependence of the conversion gain on the LO wave power when the LO wave electric power exceeds the predetermined value Po, the present invention offers another advantage of being able to reduce the amount of change in the conversion gain caused by a change in the DC characteristic resulting from a change in the temperature of each diode of the APDP. Fig. 13 shows the DC characteristic of the APDP 11 at a high temperature and a low temperature of each diode as well as the DC characteristic of the APDP 11 at a normal temperature of each diode. As previously mentioned, a rate of increase of the electric current which flows through the APDP 11 according to an increase in the terminal voltage of the APDP 11 is smaller than that of the prior art APDP 2, and the change in the electric current which flows through the APDP 11 is extremely small even if the terminal voltage changes somewhat. As a result, the electric current, which flows through the APDP 11, hardly changes if the same terminal voltage is applied to the APDP 11 even though the temperature of each diode of the APDP changes. Fig. 14 is a graph showing a change in the dependence of the conversion gain of the APDP 11 on the LO wave electric power resulting from a change in the temperature of each diode. As shown in the figure, while the conversion gain of the APDP 11 changes somewhat with a change in the temperature of each diode, the change in the conversion gain with temperature is very small when the LO wave electric power having the predetermined value Po or more is applied to the APDP.

As previously mentioned, in accordance with the first embodiment, the even harmonic mixer makes it possible to reduce the amount of change of the conversion gain resulting from a change in the electric power of an LO wave applied to the even harmonic mixer and a change in the temperature of each diode

of the APDP.

Numerous variants may be made in the first embodiment mentioned above as follows.

Fig. 15 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a variant of the first embodiment. The even harmonic mixer according to this variant is a stub demultiplexing mixer. In the figure, the same reference numerals as shown in Fig. 10 denote the same components as those of the even harmonic mixer according to the above-mentioned first embodiment or like components. Furthermore, reference numeral 12 denotes a line with an open end, having an electrical length equal to one quarter-wavelength of an LO wave applied to the even harmonic mixer, and reference numeral 13 denotes a line with a short-circuited end, having an electrical length equal to one quarter-wavelength of the LO wave.

The stub demultiplexing mixer shown in Fig. 15 is used when the frequency of an IF signal applied to the even harmonic mixer is lower than the frequency of the LO wave. At the frequency of the LO wave, the line 13 with a short-circuited end is assumed to be open when viewed from a node A between the line 13 and the APDP 11 and the line 12 with an open end is assumed to be short-circuited when viewed from a node B between the line 12 and the APDP 11. Therefore, the LO wave applied to the LO terminal 8 flows into the line 12 with an open end by way of the APDP 11. Furthermore, since the frequency of the IF signal is lower than the frequency of the LO wave, the frequency of an RF signal applied to the even harmonic mixer becomes about twice the frequency of the LO wave. Therefore, at the frequency of the RF signal, the line 13 with a short-circuited end is assumed

to be short-circuited when viewed from the node A between the line 13 and the APDP 11 and the line 12 with an open end is assumed to be open when viewed from the node B between the line 12 and the APDP 11. Therefore, the RF signal applied to the RF terminal 7 flows into the line 13 with a short-circuited end by way of the APDP 11.

Even in this variant, since the DC characteristic of the APDP 11 which consists of the first and second resistors 10a and 10b and the first and second diodes 1a and 1b connected in series to those resistors, respectively, does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode, it is possible to control the change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the first embodiment is not limited to the case. Alternatively, the first embodiment can also be applied to a case where the IF signal is a balanced signal. Fig. 16 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to another variant of the first embodiment. In the figure, reference numeral 40 denotes a HPF disposed between the APDP 11 and a ground potential, for allowing only an RF signal and an LO wave to pass therethrough, and reference numeral 6b denotes a LPF having an end connected to a node between the HPF 40 and the APDP 11, and another end connected to an inverted IF terminal 9b via which the inversion of an IF signal is input and output. The HPF 40 may be a simple circuit which consists of only a capacitor. And, the IF signal which is a balanced signal and the inversion of the IF signal are input and output

by way of the IF terminal 9a and the inverted IF terminal 9b, respectively. Even in the even harmonic mixer constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to control the change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode.

Fig. 17 is a schematic circuit diagram showing the structure of an APDP 11 according to another variant of the first embodiment. In this variant, the first and second resistors 10a and 10b are connected to the anodes of the first and second diodes 1a and 1b which constitute the APDP 11, respectively. When the APDP 11 according to this variant is applied to an even harmonic mixer, the same advantage is provided. In other words, it is possible to control the change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Fig. 18 is a schematic circuit diagram showing the structure of an APDP 11 according to another variant of the first embodiment. In this variant, the first resistor 10a is connected to the cathode of the first diode 1a and the second resistor 10b is connected to the anode of the second diode 1b. When the APDP 11 according to this variant is applied to an even harmonic mixer, the same advantage is provided. In other words, it is possible to control the change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode.

Although the number of resistors connected in series to each diode included in the APDP 11 is one in the above-mentioned

embodiment and variants, in accordance with the present invention the number of resistors is not limited to one and a plurality of resistors can be connected to each diode of the APDP. Fig. 19 is a schematic circuit diagram showing the structure of an APDP 11 according to such a variant. In this variant, the number of resistors connected in series to each diode which constitutes the APDP 11 is two, and two resistors are connected to both the anode and cathode of each diode, respectively. When the APDP 11 according to this variant is applied to an even harmonic mixer, the same advantage is provided. In other words, it is possible to control the change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Embodiment 2.

Fig. 20 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a second embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 10 denote the same components as those of the even harmonic mixer according to the above-mentioned first embodiment or like components, and the explanation of those components will be omitted hereafter. Furthermore, in Fig. 20, reference numeral 1c denotes a third diode connected in series to a first diode 1a, and reference numeral 1d denotes a fourth diode connected in series to a second diode 1b. Thus, in an APDP 11 according to the second embodiment, a first series unit which consists of the two diodes 1a and 1c connected in series (cascaded) and a first resistor 10a connected in series to those diodes 1a and 1c, and a second series unit which consists of the two remaining diodes 1b and 1d connected

in series and a second resistor 10b connected in series to those diodes 1b and 1d are connected in parallel so that the first set of diodes 1a and 1c and the second set of diodes 1b and 1d are opposite in polarity.

Next, a description will be made as to the operation of the even harmonic mixer according to the second embodiment.

The APDP 11 incorporated into the even harmonic mixer according to the second embodiment operates basically in the same way that the APDP 11 according to the above-mentioned first embodiment does. Therefore, only a characterized operation of the even harmonic mixer according to the second embodiment will be explained in the following.

Since two diodes are cascaded in each series unit of the APDP 11, the terminal voltage applied to each diode stage included in each series unit is reduced to half that across each diode included in each series unit of the APDP of the even harmonic mixer of the first embodiment. In general, distortion to be created in a diode grows nonlinearly as the terminal voltage applied to the diode increases. Therefore, it is possible to reduce the amount of distortion to be created when the level of an input signal is increased as compared with the case where only one diode is provided in each series unit. In other words, an excellent distortion characteristic is acquired.

Furthermore, needless to say that even in the even harmonic mixer which employs the APDP 11 constructed as above, since the APDP 11 shows a DC characteristic that does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, like the APDP of the above-mentioned first embodiment, it is possible to reduce the amount of change in the conversion gain resulting from the change

in the LO wave electric power and the change in the temperature of each diode of the APDP.

The number of diodes cascaded in each series unit which constitutes the APDP 11 is not limited to two, and the APDP 11 can alternatively be comprised of two series units in each of which three or more diodes are cascaded. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased.

Embodiment 3.

Fig. 21 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a third embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 10 denote the same components as those of the even harmonic mixer according to the above-mentioned first embodiment or like components, and the explanation of those components will be omitted hereafter. Furthermore, in Fig. 21, reference numeral 14a denotes a first capacitor connected in parallel to a first resistor 10a connected in series to a first diode 1a, and reference numeral 14b denotes a second capacitor connected in parallel to a second resistor 10b connected in series to a second diode 1b. Thus, in an APDP 11 according to the third embodiment, a first series unit which consists of the first diode 1a and the first resistor 10a connected in series, and the first capacitor 14a connected in parallel to the first resistor 10a, and a second series unit which consists of the second diode 1b and the second resistor 10b connected in series, and the second capacitor 14b connected in parallel to the second resistor 10b are connected in parallel so that the first and second diodes 1a and 1b are opposite in polarity.

Next, the operation of the even harmonic mixer according to the third embodiment will be explained.

The description will be made assuming that the even harmonic mixer is the one intended for reception, and an RF signal and an LO wave are applied to an RF terminal 7 and an LO terminal LO 8, respectively, and an IF signal is extracted from an IF terminal 9. The APDP 11 incorporated into the even harmonic mixer according to the third embodiment operates basically in the same way that the APDP 11 according to the above-mentioned first embodiment does. Therefore, only a characterized operation of the even harmonic mixer of the third embodiment will be explained in the following.

Fig. 22 is a diagram for explaining a flow of an RF signal in the APDP 11 according to the third embodiment. Not only an LO wave but also an RF signal should be applied to the APDP 11 when the even harmonic mixer operates as a mixer for reception. When the even harmonic mixer does not include the first and second capacitors 14a and 14b (that is, in the case of the above-mentioned first embodiment shown in Fig. 10), a voltage drop is caused in either the first resistor 10a or the second resistor 10b connected in series to each diode when an RF signal is applied to the APDP 11, and this results in a decrease in the voltage of the RF signal applied to each diode. As a result, the conversion gain is reduced.

In contrast, in the APDP 11 according to the third embodiment shown in Fig. 22, the RF signal applied to the APDP passes through the second capacitor 14b other than the second resistor 10b in positive cycles of the RF signal. On the other hand, the RF signal passes the first capacitor 14a other than the first resistor 10a in negative cycles of the RF signal. As

a result, since no voltage drop is caused because of the first resistor 10a or the second resistor 10b, it is possible to reduce the amount of change in the conversion gain resulting from a change in the LO wave electric power of the even harmonic mixer and a change in the temperature of each diode of the APDP without causing a decrease in the conversion gain.

The even harmonic mixer according to the third embodiment can be used as a mixer for transmission in which an IF signal is input and an RF signal and an LO wave are output. In this case, the same advantage is provided.

Numerous variants may be made in the third embodiment mentioned above as follows.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the third embodiment is not limited to the case. Alternatively, the third embodiment can also be applied to a case where the IF signal is a balanced signal. Fig. 23 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to a variant of the third embodiment. In the figure, reference numeral 40 denotes a HPF disposed between the APDP 11 and a ground potential, for allowing only an RF signal and an LO wave to pass therethrough, and reference numeral 6b denotes a LPF having an end connected to a node between the HPF 40 and the APDP 11, and another end connected to an inverted IF terminal 9b. The HPF 40 may be a simple circuit which consists of only a capacitor. And, the IF signal which is a balanced signal and the inversion of the IF signal are input and output by way of the IF terminal 9a and the inverted IF terminal 9b. Even in the even harmonic mixer constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a

change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode.

In another variant of the third embodiment, both first and second resistors 10a and 10b and first and second capacitors 14a and 14b are connected to anodes of the first and second diodes 1a and 1b which constitute the APDP 11, respectively. When the APDP 11 according to this variant is applied to an even harmonic mixer, the same advantage is provided. In other words, it is possible to reduce the amount of change in the conversion gain resulting from a change in the LO wave electric power and a change in the temperature of each diode of the APDP.

Furthermore, in another variant of the third embodiment, a first resistor 10a and a first capacitor 14a are connected to an anode of the first diode 1a, and a second resistor 10b and a second capacitor 14b are connected to a cathode of the second diode 1b. When the APDP 11 according to this variant is applied to an even harmonic mixer, the same advantage is provided. In other words, it is possible to reduce the amount of change in the conversion gain resulting from a change in the LO wave electric power and a change in the temperature of each diode of the APDP.

Furthermore, in another variant of the third embodiment, a parallel circuit in which a resistor and a capacitor are connected in parallel is connected to each of the anode and cathode of the first diode 1a, and a parallel circuit in which a resistor and a capacitor are connected in parallel is connected to each of the anode and cathode of the second diode 1b. When the APDP

11 according to this variant is applied to an even harmonic mixer, the same advantage is provided. In other words, it is possible to reduce the amount of change in the conversion gain resulting from a change in the LO wave electric power and a change in the temperature of each diode of the APDP.

Although the number of diodes included in each series unit which constitutes the APDP 11 is one in the above-mentioned third embodiment and variants, the number of diodes is not limited to one and two or more diodes can be cascaded in each series unit of the APDP 11. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased, as previously mentioned in Embodiment 2.

Embodiment 4.

Fig. 24 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a fourth embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 10 denote the same components as those of the even harmonic mixer according to the above-mentioned first embodiment or like components, and the explanation of those components will be omitted hereafter. Furthermore, in Fig. 24, reference numeral 15a denotes a first capacitor having an end connected to a node between a cathode of a first diode 1a and a first resistor 10a, and reference numeral 15b denotes a second capacitor having an end connected to a node between an anode of a second diode 1b and a second resistor 10b. In an APDP 11 according to the fourth embodiment, the first resistor 10a is connected to the cathode of the first diode 1a in a first series unit and the second resistor 10b is connected

to the anode of the second diode 1b in a second series unit so that the first and second resistors 10a and 10b are connected to each other at an end of the APDP 11.

The other ends of the first and second capacitors 15a and 15b are connected to each other, and furthermore, a node between them is connected to an RF terminal 7 by way of a HPF 4 and is also connected to an LO terminal 8 by way of a BPF 5. Furthermore, a node between the first and second resistors 10a and 10b is connected to an IF terminal 9. Each of the first and second capacitors 15a and 15b has a capacitance that is set to a value to allow an RF signal and an LO wave to pass therethrough and to block an IF signal.

Next, the operation of the even harmonic mixer according to the fourth embodiment will be explained.

The description will be made assuming that the even harmonic mixer is the one intended for reception, and an RF signal and an LO wave are applied to the RF terminal 7 and the LO terminal 8, respectively, and an IF signal is extracted from the IF terminal 9. Fig. 25 shows a flow of the RF signal in the APDP 11 according to the fourth embodiment. The RF signal applied to the APDP 11 passes through the first capacitor 15a or the second capacitor 15b, and then enters the first diode 1a or the second diode 1b. Therefore, any voltage drop in the RF signal according to the resistor connected in series to each diode is not caused, as in the case of the third embodiment. On the other hand, since a direct current is blocked by the first and second capacitors 15a and 15b, a parallel circuit constructed of the first series unit which consists of the first diode 1a and the first resistor 10a and the second series unit which consists of the second diode 1b and the second resistor 10b, operates like the APDP according

to the above-mentioned first embodiment. Therefore, even in the even harmonic mixer which employs the APDP 11 constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

In addition, since the IF signal generated by the first diode 1a or the second diode 1b is blocked by the first and second capacitors 15a and 15b, the IF signal is output by way of the IF terminal 9 connected to the node between the first and second resistors 10a and 10b. At this time, the RF signal is blocked by the first and second resistors 10a and 10b and does not appear at the IF terminal 9 because the impedance of each of the first and second capacitors 15a and 15b is smaller than the resistance of each of the first and second resistors 10a and 10b. Therefore, a LPF for allowing only an IF signal to pass therethrough, which is needed in the above-mentioned embodiments, becomes unnecessary.

The even harmonic mixer according to the fourth embodiment is available as a mixer for transmission which inputs an IF signal and outputs an RF signal and an LO wave, and offers the same advantages.

Numerous variants may be made in the fourth embodiment mentioned above as follows.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the fourth embodiment is not limited to the case. Alternatively, the fourth embodiment can also be applied to a case where the IF signal is a balanced

signal. Fig. 26 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to a variant of the fourth embodiment. In the figure, reference numeral 40 denotes a HPF disposed between the APDP 11 and a ground potential, for allowing only an RF signal and an LO wave to pass therethrough, and reference numeral 6b denotes a LPF having an end connected to a node between the HPF 40 and the APDP 11, and another end connected to an inverted IF terminal 9b. The HPF 40 may be a simple circuit which consists of only a capacitor. And, the IF signal which is a balanced signal and the inversion of the IF signal are input and output by way of the IF terminal 9a and the inverted IF terminal 9b. Since the even harmonic mixer according to this variant operates like the even harmonic mixer of Fig.16 and the APDP 11 shows a DC characteristic that does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, like that as shown in Fig. 24, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Although the number of diodes included in each series unit which constitutes the APDP 11 is one in the above-mentioned fourth embodiment and variants, the number of diodes is not limited to one and two or more diodes can be cascaded in each series unit of the APDP. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased.

Embodiment 5.

Fig. 27 is a schematic circuit diagram showing the

structure of an even harmonic mixer according to a fifth embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 21 denote the same components as those of the even harmonic mixer according to the above-mentioned third embodiment or like components, and the explanation of those components will be omitted hereafter. In an APDP 11 according to the fifth embodiment, a first resistor 10a is connected to a cathode of a first diode 1a in a first series unit of the APDP and a second resistor 10b is connected to an anode of a second diode 1b in a second series unit of the APDP so that the first and second resistors 10a and 10b are connected to each other at an end of the APDP. Furthermore, a first capacitor 14a is connected in parallel to the first resistor 10a and a second capacitor 14b is connected in parallel to the first resistor 10b. A node between the first and second resistors 10a and 10b is connected to an IF terminal 9.

Furthermore, in Fig. 27, reference numeral 15a denotes a third capacitor having an end connected to a node between the cathode of the first diode 1a and the first resistor 10a, and reference numeral 15b denotes a fourth capacitor having an end connected to a node between the anode of the second diode 1b and the second resistor 10b. The other ends of the third and fourth capacitors 15a and 15b are connected to each other, and a node between them is connected to an RF terminal 7 by way of a HPF 4 and is also connected to an LO terminal 8 by way of a BPF 5. Each of the first and second capacitors 14a and 14b has a capacitance that is set to allow an IF signal to pass therethrough, and each of the third and fourth capacitors 15a and 15b has a capacitance that is set to allow an RF signal and an LO wave to pass therethrough, and to block the IF signal.

Next, the operation of the even harmonic mixer according to the fifth embodiment will be explained.

The description will be made assuming that the even harmonic mixer is the one intended for reception, and an RF signal and an LO wave are applied to the RF terminal 7 and the LO terminal 8, respectively, and an IF signal is extracted from the IF terminal 9. In the above-mentioned fourth embodiment shown in Fig. 24, the IF signal passes through the first resistor 10a or the second resistor 10b and is output to the IF terminal 9. Therefore, the IF signal may be attenuated because of the first resistor 10a or the second resistor 10b. In contrast, in the fifth embodiment, since the first and second capacitors 14a and 14b are connected in parallel to the first and second resistors 10a and 10b, respectively, the IF signal is output to, by way of the IF terminal 9, outside the mixer without being attenuated because of the first and second resistors 10a and 10b by setting the capacitance of each of the first and second capacitors 14a and 14b to a value to allow the IF signal to pass therethrough.

Thus, neither the first capacitor 14a nor the second capacitor 14b has an influence on the electric currents which flow through the first diode 1a and the second diode 1b included in the two series units of the APDP 11, respectively, and therefore the electric currents which flow through the first diode 1a and the second diode 1b can be kept constant with the first resistor 10a or the second resistor 10b. Thus, even in the even harmonic mixer which employs the APDP 11 constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in

the LO wave electric power and the change in the temperature of each diode of the APDP.

The even harmonic mixer according to the fifth embodiment is available as a mixer for transmission which inputs an IF signal and outputs both an RF signal and an LO wave, and offers the same advantages.

Numerous variants may be made in the fifth embodiment mentioned above as follows.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the fifth embodiment is not limited to the case. Alternatively, the fifth embodiment can also be applied to a case where the IF signal is a balanced signal. Fig. 28 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to a variant of the fifth embodiment. In the figure, reference numeral 40 denotes a HPF disposed between the APDP 11 and a ground potential, for allowing only an RF signal and an LO wave to pass therethrough, and reference numeral 6b denotes a LPF having an end connected to a node between the HPF 40 and the APDP 11, and another end connected to an inverted IF terminal 9b. The HPF 40 may be a simple circuit which consists of only a capacitor. And, the IF signal which is a balanced signal and the inversion of the IF signal are input and output by way of the IF terminal 9a and the inverted IF terminal 9b. Since the even harmonic mixer according to this variant operates like the even harmonic mixer of Fig. 16 and the APDP 11 shows a DC characteristic that does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, like that as shown in Fig. 27, it is possible to reduce the amount of change in the conversion

gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Although the number of diodes included in each series unit which constitutes the APDP 11 is one in the above-mentioned fifth embodiment and variants, the number of diodes is not limited to one and two or more diodes can be cascaded in each series unit of the APDP. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased, as mentioned in Embodiment 2.

Embodiment 6.

Fig. 29 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a sixth embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 10 denote the same components as those of the even harmonic mixer according to the above-mentioned first embodiment or like components, and the explanation of those components will be omitted hereafter. In an APDP 11 according to the sixth embodiment, a first resistor 10a is connected to a cathode of a first diode 1a in a first series unit of the APDP and a second resistor 10b is connected to an anode of a second diode 1b in a second series unit of the APDP so that the first and second resistors 10a and 10b are connected to each other at an end of the APDP.

Furthermore, in Fig. 29, reference numeral 17a denotes a first capacitor having an end connected in series to an anode of the first diode 1a, reference numeral 17b denotes a second capacitor having an end connected in series to a cathode of the second diode 1b, reference numeral 18a denotes a third capacitor having an end connected to a node between the cathode of the

first diode 1a and the first resistor 10a, reference numeral 18b denotes a fourth capacitor having an end connected to a node between the anode of the second diode 1b and the second resistor 10b, reference numeral 19a denotes a third resistor having an end connected to a node between the anode of the first diode 1a and the first capacitor 17a, and reference numeral 19b denotes a fourth resistor having an end connected to a node between the cathode of the second diode 1b and the second capacitor 17b. The other ends of the first and second capacitors 17a and 17b are connected to each other and a node between them is connected to a ground potential. The first and second resistors 10a and 10b are connected to each other and a node between them is connected to an IF terminal 9a. The third and fourth resistors 19a and 19b are connected to each other and a node between them is connected to an inverted IF terminal 9b. The other ends of the third and fourth capacitors 18a and 18b are connected to other, and a node between them is connected to an RF terminal 7 by way of a HPF 4 and is also connected to an LO terminal 8 by way of a BPF 5. Each of the first and second capacitors 17a and 17b and the third and fourth capacitors 18a and 18b has a capacitance set to a value which allows an RF signal and an LO wave to pass therethrough and blocks an IF signal.

Next, the operation of the even harmonic mixer according to the sixth embodiment will be explained.

The description will be made assuming that the even harmonic mixer is the one intended for reception in which an RF signal and an LO wave are applied to the RF terminal 7 and the LO terminal 8, respectively, and an IF signal and the inversion of the IF signal are extracted from the IF terminal 9a and the inverted IF terminal 9b, respectively.

The RF signal applied to the RF terminal 7 is input to the APDP 11 by way of the HPF 4. The input RF signal is then furnished to either the first diode 1a or the second diode 1b by way of the third capacitor 18a or the fourth capacitor 18b, and further reaches the ground potential by way of either the first capacitor 17a or the second capacitor 17b. Therefore, any voltage drop in the RF signal is not caused because of the first through fourth resistors 10a, 10b, 19a, and 19b. On the other hand, since a direct current is blocked by the first through fourth capacitors 17a, 17b, 18a, and 18b, a parallel circuit, which consists of a series unit (which differs from the first series unit) in which the first diode 1a and the first and third resistors 10a and 19a are connected to each other and another series unit (which differs from the second series unit) in which the second diode 1b and the second and fourth resistors 10b and 19b are connected to each other, operates like the APDP according to the above-mentioned first embodiment. Therefore, even in the even harmonic mixer which employs the APDP 11 constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Furthermore, because the IF signal generated by either the first diode 1a or the second diode 1b is blocked by the first and second capacitors 17a and 17b and the third and fourth capacitors 18a and 18b, the IF signal and the inversion of the IF signal are output from a node between the first and second resistors 10a and 10b and a node between the third and fourth

resistors 19a and 19b, respectively. At this time, the RF signal is blocked by the first through fourth resistors 10a, 10b, 19a, and 19b and does not appear at the IF terminal 9a and the inverted IF terminal 9b because each of the first through fourth capacitors 17a, 17b, 18a, and 18b has an impedance smaller than the resistance of each of the first through fourth resistors 10a, 10b, 19a, and 19b. Therefore, the even harmonic mixer of the sixth embodiment makes it possible to output the IF signal as a balanced signal even if there is no low-pass filter that allows only IF signals to pass therethrough, though such a low-pass filter is needed in the first through third embodiments mentioned above.

The even harmonic mixer according to the sixth embodiment is available as a mixer for transmission which inputs an IF signal and outputs both an RF signal and an LO wave, and offers the same advantages.

Numerous variants may be made in the sixth embodiment mentioned above as follows.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the sixth embodiment is not limited to the case. Alternatively, the sixth embodiment can also be applied to a case where the IF signal is a balanced signal. Fig. 30 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to a variant of the sixth embodiment. In this variant, the inverted IF terminal 9b connected to the node between the third and fourth resistors 19a and 19b is removed, the first resistor 10a, the first diode 1a, and the first capacitor 17a are connected in series in the first series unit, and the second resistor 10b, the second diode 1b, and the second capacitor 17b are connected in series in the second series unit. As a

result, the IF signal is input and output as an unbalanced signal only to and from the IF terminal 9. Even in this variant, since the APDP 11 shows a DC characteristic that does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, like that as shown in Fig. 27, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Although the number of diodes included in each series unit which constitutes the APDP 11 is one in the above-mentioned sixth embodiment and variants, the number of diodes is not limited to one and two or more diodes can be cascaded in each series unit of the APDP. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased, as mentioned in Embodiment 2.

Embodiment 7.

Fig. 31 is a schematic circuit diagram showing the structure of an even harmonic mixer according to a seventh embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 10 denote the same components as those of the even harmonic mixer according to the above-mentioned first embodiment or like components, and the explanation of those components will be omitted hereafter. In an APDP 11 according to the seventh embodiment, a first resistor 10a is connected to a cathode of a first diode 1a in a first series unit of the APDP and a second resistor 10b is connected to an anode of a second diode 1b in a second series unit of the APDP so that the first and second resistors 10a and 10b are

connected to each other at an end of the APDP 11.

Furthermore, in Fig. 31, reference numeral 10c denotes a third resistor having an end connected in series to an anode of the first diode 1a, reference numeral 10d denotes a fourth resistor having an end connected in series to a cathode of the second diode 1b, reference numeral 16a denotes a first capacitor connected in parallel to the third resistor 10c, reference numeral 16b denotes a second capacitor connected in parallel to the fourth resistor 10d, reference numeral 18a denotes a third capacitor having an end connected to a node between the cathode of the first diode 1a and the first resistor 10a, and reference numeral 18b denotes a fourth capacitor having an end connected to a node between the anode of the second diode 1b and the second resistor 10b. The first and second resistors 10a and 10b are connected to each other and a node between them is connected to an IF terminal 9a. The other ends of the third and fourth resistors 10c and 10d is connected to each other, and a node between them is connected to an inverted IF terminal 9b by way of a LPF 6 and is also connected to a ground potential by way of a HPF 40. The other ends of the third and fourth capacitors 18a and 18b are connected to each other, and a node between them is connected to an RF terminal 7 by way of the HPF 40 and is also connected to an LO terminal 8 by way of a BPF 5. Each of the first through fourth capacitors 16a, 16b, 18a, and 18b has a capacitance set to a value which allows an RF signal and an LO wave to pass therethrough and blocks an IF signal.

Next, the operation of the even harmonic mixer according to the seventh embodiment will be explained.

The description will be made assuming that the even harmonic mixer is the one intended for reception in which an

RF signal and an LO wave are applied to the RF terminal 7 and the LO terminal 8, respectively, and an IF signal and the inversion of the IF signal are extracted from the IF terminal 9a and the inverted IF terminal 9b, respectively.

The RF signal applied to the RF terminal 7 is input to the APDP 11 by way of the HPF 40. The input RF signal is then furnished to either the first diode 1a or the second diode 1b by way of the third capacitor 18a or the fourth capacitor 18b, and further reaches the ground potential by way of either the first capacitor 16a or the second capacitor 16b and by way of the HPF 40. Therefore, any voltage drop in the RF signal is not caused because of the first through fourth resistors 10a, 10b, 10c, and 10d. On the other hand, since a direct current is blocked by the third and fourth capacitors 18a and 18b, a parallel circuit, which consists of the first series unit in which the first diode 1a and the first and third resistors 10a and 10c are connected to each other and the second series unit in which the second diode 1b and the second and fourth resistors 10b and 10d are connected to each other, operates like the APDP according to the above-mentioned first embodiment. Therefore, even in the even harmonic mixer which employs the APDP 11 constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Furthermore, because the IF signal generated by either the first diode 1a or the second diode 1b is blocked by the first through fourth capacitors 16a, 16b, 18a and 18b, the IF signal

and the inversion of the IF signal are output from a node between the first and second resistors 10a and 10b and a node between the third and fourth resistors 10c and 10d, respectively. At this time, the RF signal is blocked by the first through fourth resistors 10a, 10b, 10c, and 10d and does not appear at the IF terminal 9a and the inverted IF terminal 9b because each of the first through fourth capacitors 16a, 16b, 18a, and 18b has an impedance smaller than the resistance of each of the first through fourth resistors 10a, 10b, 10c, and 10d. Therefore, the even harmonic mixer of the seventh embodiment makes it possible to output the IF signal as a balanced signal even if there is no low-pass filter that allows only IF signals to pass therethrough, though such a low-pass filter is needed in the first through third embodiments mentioned above.

The even harmonic mixer according to the seventh embodiment is available as a mixer for transmission which inputs an IF signal and outputs both an RF signal and an LO wave, and offers the same advantages.

Numerous variants may be made in the seventh embodiment mentioned above as follows.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the seventh embodiment is not limited to the case. Alternatively, the seventh embodiment can also be applied to a case where the IF signal is a balanced signal. Fig. 32 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to a variant of the seventh embodiment. In this variant, the inverted IF terminal 9b connected, by way of the LPF 6, to the node between the third and fourth resistors 10c and 10d is removed. As a

result, the IF signal is input and output as an unbalanced signal only to and from the IF terminal 9. Even in this variant, since the APDP 11 shows a DC characteristic that does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, like that as shown in Fig. 27, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Although the number of diodes included in each series unit which constitutes the APDP 11 is one in the above-mentioned seventh embodiment and variants, the number of diodes is not limited to one and two or more diodes can be cascaded in each series unit of the APDP. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased, as mentioned in Embodiment 2.

Embodiment 8.

Fig. 33 is a schematic circuit diagram showing the structure of an even harmonic mixer according to an eighth embodiment of the present invention. In the figure, the same reference numerals as shown in Fig. 21 denote the same components as those of the even harmonic mixer according to the above-mentioned third embodiment or like components, and the explanation of those components will be omitted hereafter. In an APDP 11 according to the eighth embodiment, a first resistor 10a is connected to a cathode of a first diode 1a in a first series unit of the APDP and a second resistor 10b is connected to an anode of a second diode 1b in a second series unit of the

APDP so that the first and second resistors 10a and 10b are connected to each other at an end of the APDP 11. A first capacitor 14a is connected in parallel to the first resistor 10a, and a second capacitor 14b is connected in parallel to the second resistor 10b.

Furthermore, in Fig. 33, reference numeral 20a denotes a third capacitor having an end connected in series to an anode of the first diode 1a, reference numeral 20b denotes a fourth capacitor having an end connected in series to a cathode of the second diode 1b, reference numeral 21a denotes a third resistor having an end connected to a node between the anode of the first diode 1a and the third capacitor 20a, and reference numeral 21b denotes a fourth resistor having an end connected to a node between the cathode of the second diode 1b and the fourth capacitor 20b. A node between the first and second resistors 10a and 10b is connected to an RF terminal 7 by way of a HPF 4, an LO terminal 8 by way of a BPF 5, and an IF terminal 9a by way of the LPF 6. The other ends of the third and fourth resistors 21a and 21b is connected to each other, and a node between them is connected to an inverted IF terminal 9b. The other ends of the third and fourth capacitors 20a and 20b are connected to each other, and a node between them is connected to a ground potential. Each of the first through fourth capacitors 14a, 14b, 20a, and 20b has a capacitance set to a value which allows an RF signal and an LO wave to pass therethrough and blocks an IF signal.

Next, the operation of the even harmonic mixer according to the eighth embodiment will be explained.

The description will be made assuming that the even harmonic mixer is the one intended for reception in which an RF signal and an LO wave are applied to the RF terminal 7 and

the LO terminal 8, respectively, and an IF signal and the inversion of the IF signal are extracted from the IF terminal 9a and the inverted IF terminal 9b, respectively.

The RF signal applied to the RF terminal 7 is input to the APDP 11 by way of the HPF 4. The input RF signal is then furnished to either the first diode 1a or the second diode 1b by way of the first capacitor 14a or the second capacitor 14b, and further reaches the ground potential by way of either the third capacitor 20a or the fourth capacitor 20b. Therefore, any voltage drop in the RF signal is not caused because of the first through fourth resistors 10a, 10b, 21a, and 21b. On the other hand, since a direct current is blocked by the third and fourth capacitors 20a and 20b, a parallel circuit, which consists of the first series unit in which the first diode 1a and the first and third resistors 10a and 21a are connected to each other and the second series unit in which the second diode 1b and the second and fourth resistors 10b and 21b are connected to each other, operates like the APDP according to the above-mentioned first embodiment. Therefore, even in the even harmonic mixer which employs the APDP 11 constructed as above, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Furthermore, because the IF signal generated by either the first diode 1a or the second diode 1b is blocked by the first through fourth capacitors 14a, 14b, 20a and 20b, the IF signal and the inversion of the IF signal are output from a node between

the first and second resistors 10a and 10b and a node between the third and fourth resistors 21a and 21b, respectively. At this time, the RF signal is blocked by the first through fourth resistors 10a, 10b, 21a, and 21b and does not appear at the IF terminal 9a and the inverted IF terminal 9b because each of the first through fourth capacitors 14a, 14b, 20a, and 20b has an impedance smaller than the resistance of each of the first through fourth resistors 10a, 10b, 21a, and 21b. Therefore, the even harmonic mixer of the eighth embodiment makes it possible to output the IF signal as a balanced signal even if there is no low-pass filter that allows only IF signals to pass therethrough, though such a low-pass filter is needed in the first through third embodiments mentioned above.

The even harmonic mixer according to the eighth embodiment is available as a mixer for transmission which inputs an IF signal and outputs both an RF signal and an LO wave, and offers the same advantages.

Numerous variants may be made in the eighth embodiment mentioned above as follows.

Although it is assumed that the IF signal is an unbalanced signal in the above-mentioned explanation, the eighth embodiment is not limited to the case. Alternatively, the eighth embodiment can also be applied to a case where the IF signal is a balanced signal. Fig. 34 is a schematic circuit diagram showing the structure of an even harmonic mixer for mixing an IF signal which is a balanced signal according to a variant of the eighth embodiment. In this variant, the inverted IF terminal 9b connected to the node between the third and fourth resistors 21a and 21b is removed, the first resistor 10a, the first diode 1a, and the third capacitor 20a are connected in series in the

first series unit, and the second resistor 10b, the second diode 1b, and the fourth capacitor 20b are connected in series in the second series unit. As a result, the IF signal is input and output as an unbalanced signal only to and from the IF terminal 9a. Even in this variant, since the DC characteristic of the APDP 11 does not greatly depend on a change in the LO wave electric power and a change in the temperature of each diode of the APDP, it is possible to reduce the amount of change in the conversion gain resulting from the change in the LO wave electric power and the change in the temperature of each diode of the APDP.

Although the number of diodes included in each series unit which constitutes the APDP 11 is one in the above-mentioned eighth embodiment and variants, the number of diodes is not limited to one and two or more diodes can be cascaded in each series unit of the APDP. This variant makes it possible to further reduce the amount of distortion to be created when the level of an input signal is increased, as mentioned in Embodiment 2.

Industrial Applicability

As mentioned above, the even harmonic mixer in accordance with the present invention is suitable for a quadrature modulator and a quadrature demodulator for use in transmitter-receivers of a radio communications system.

WHAT IS CLAIMED IS:

1. An even harmonic mixer comprising:

an antiparallel diode pair means including a first series unit in which a first diode and a first resistor are connected in series and a second series unit in which a second diode and a second resistor are connected in series, said first and second series units being connected in parallel so that said first and second diodes are opposite in polarity.

2. The even harmonic mixer according to Claim 1, wherein said first series unit has a plurality of diodes in series which are connected in series to said first resistor and which includes said first diode, and said second series unit has a plurality of diodes in series which are connected in series to said second resistor and which includes said second diode.

3. The even harmonic mixer according to Claim 1, wherein said first series unit has a first capacitor connected in parallel to said first resistor and said second series unit has a second capacitor connected in parallel to said second resistor.

4. The even harmonic mixer according to Claim 1, wherein said first resistor is connected to a cathode of said first diode in said first series unit and said second resistor is connected to an anode of said second diode in said second series unit so that said first and second resistors are connected to each other at an end of said antiparallel diode pair means, and wherein said even harmonic mixer comprises a first capacitor having an end connected to a node between said first resistor and said

first diode and a second capacitor having an end connected to a node between said second resistor and said second diode, an IF signal is input and output by way of a node between said first and second resistors, other ends of said first and second capacitors are connected to each other, an LO wave is applied to a node between the other ends of said first and second capacitors, and an RF signal is input and output by way of the node between the other ends of said first and second capacitors.

5. The even harmonic mixer according to Claim 3, wherein said first resistor is connected to a cathode of said first diode in said first series unit and said second resistor is connected to an anode of said second diode in said second series unit so that said first and second resistors are connected to each other at an end of said antiparallel diode pair means, and wherein said even harmonic mixer comprises a third capacitor having an end connected to a node between said first resistor and said first diode and a fourth capacitor having an end connected to a node between said second resistor and said second diode, an IF signal is input and output by way of a node between said first and second resistors, other ends of said third and fourth capacitors are connected to each other, an LO wave is applied to a node between the other ends of said third and fourth capacitors, and an RF signal is input and output by way of the node between the other ends of said third and fourth capacitors.

6. The even harmonic mixer according to Claim 1, wherein said first resistor is connected to a cathode of said first diode in said first series unit and said second resistor is connected to an anode of said second diode in said second series unit so

that said first and second resistors are connected to each other at an end of said antiparallel diode pair means, and said first series unit comprises a first capacitor connected to an anode of said first diode and said second series unit comprises a second capacitor connected to a cathode of said second diode, and wherein said even harmonic mixer comprises a third resistor having an end connected to the anode of said first diode, a fourth resistor having an end connected to the cathode of said second diode and another end connected to another end of said third resistor, a third capacitor having an end connected to a node between said first resistor and said first diode, and a fourth capacitor having an end connected to a node between said second resistor and said second diode, an IF signal is input and output by way of a node between said first and second resistors, other ends of said third and fourth capacitors are connected to each other, an LO wave is applied to a node between the other ends of said third and fourth capacitors, and an RF signal is input and output by way of the node between the other ends of said third and fourth capacitors.

7. The even harmonic mixer according to Claim 1, wherein said first resistor is connected to a cathode of said first diode in said first series unit and said second resistor is connected to an anode of said second diode in said second series unit so that said first and second resistors are connected to each other at an end of said antiparallel diode pair means, and said first series unit comprises a third resistor connected in series to an anode of said first diode and a first capacitor connected in parallel to said third resistor and said second series unit comprises a fourth resistor connected in series to a cathode

of said second diode and a second capacitor connected in parallel to said fourth resistor, and wherein said even harmonic mixer comprises a third capacitor having an end connected to a node between said first resistor and said first diode and a fourth capacitor having an end connected to a node between said second resistor and said second diode, an IF signal is input and output by way of a node between said first and second resistors, other ends of said third and fourth capacitors are connected to each other, an LO wave is applied to a node between the other ends of said third and fourth capacitors, and an RF signal is input and output by way of the node between the other ends of said third and fourth capacitors.

8. The even harmonic mixer according to Claim 3, wherein said first resistor is connected to a cathode of said first diode in said first series unit and said second resistor is connected to an anode of said second diode in said second series unit so that said first and second resistors are connected to each other at an end of said antiparallel diode pair means, and said first series unit comprises a third capacitor connected in series to an anode of said first diode and said second series unit comprises a fourth capacitor connected in series to a cathode of said second diode, and wherein said even harmonic mixer comprises a third resistor having an end connected to the anode of said first diode and a fourth resistor having an end connected to the cathode of said second diode and another end connected to another end of said third resistor.

Abstract

An even harmonic mixer comprises an antiparallel diode pair unit (11) including a first series unit in which a first diode (1a) and a first resistor (10a) are connected in series and a second series unit in which a second diode (1b) and a second resistor (10b) are connected in series, the first and second series units being connected in parallel so that the first and second diodes are opposite in polarity.

FIG.1

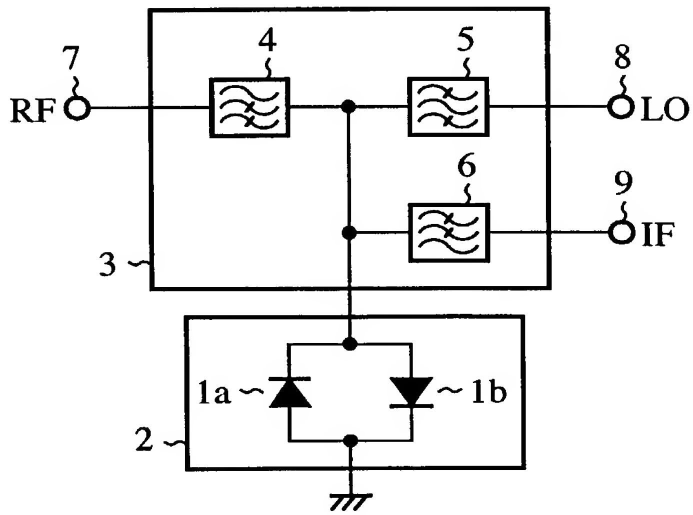


FIG.2

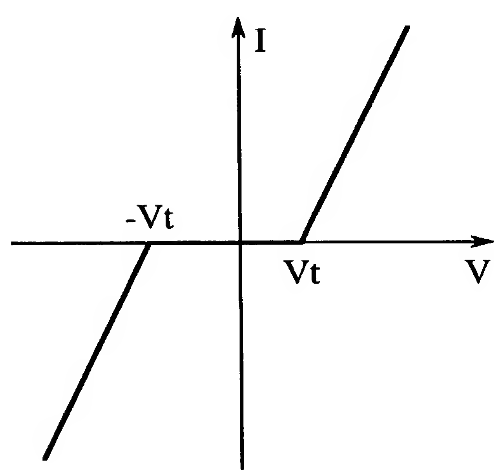


FIG.3

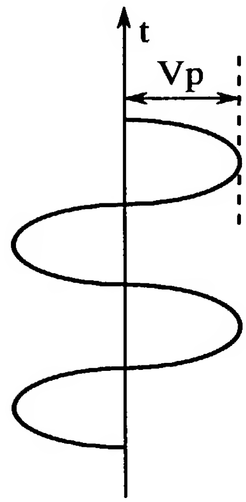


FIG.4

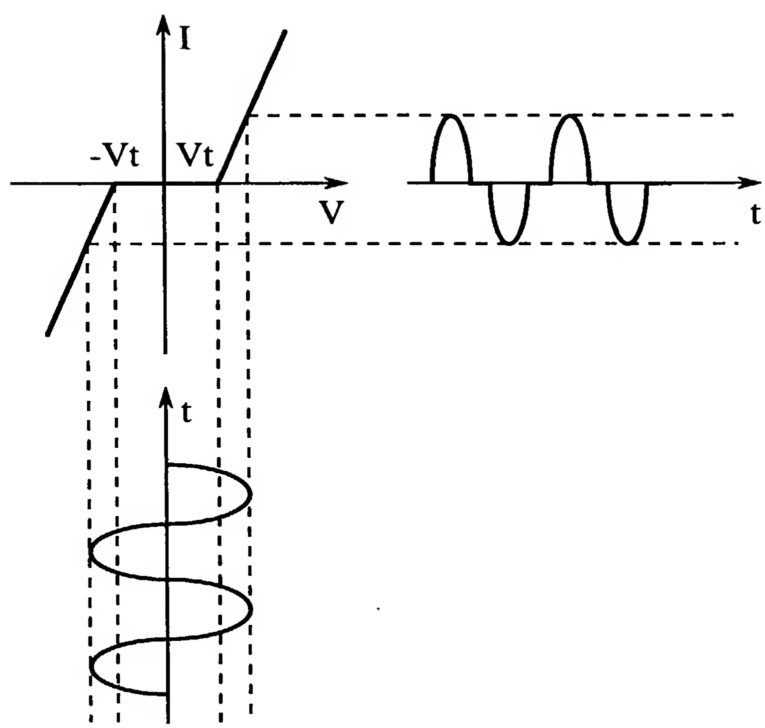
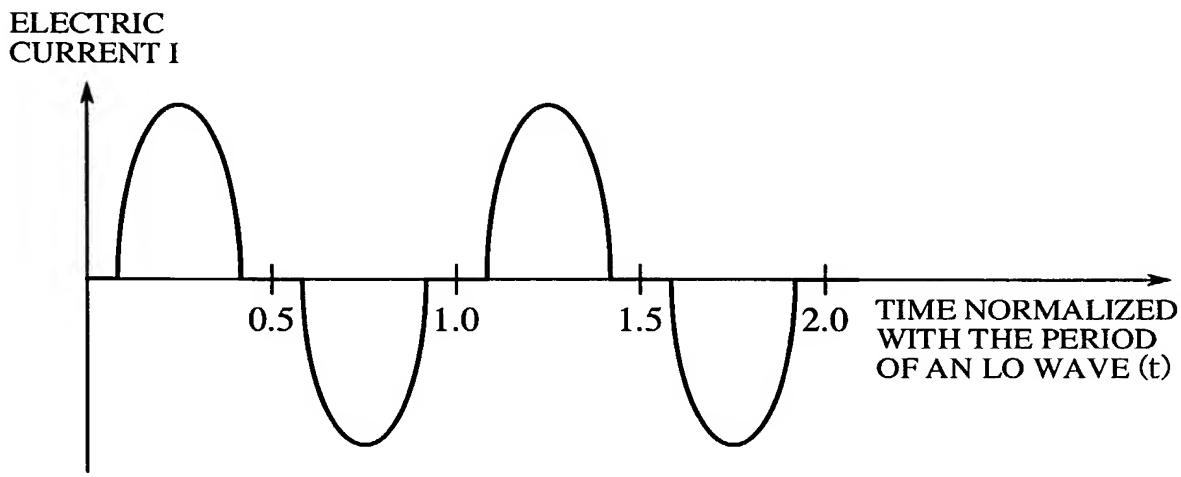


FIG.5

(a)


ELECTRIC
CURRENT I
0.5
1.0
1.5
2.0
TIME NORMALIZED
WITH THE PERIOD
OF AN LO WAVE (t)

(b)

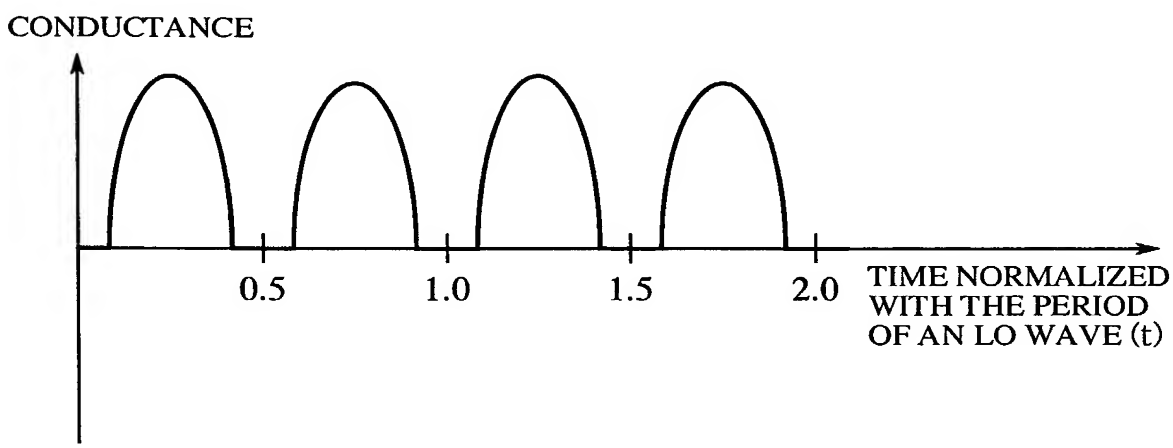

CONDUCTANCE
0.5
1.0
1.5
2.0
TIME NORMALIZED
WITH THE PERIOD
OF AN LO WAVE (t)

FIG.6

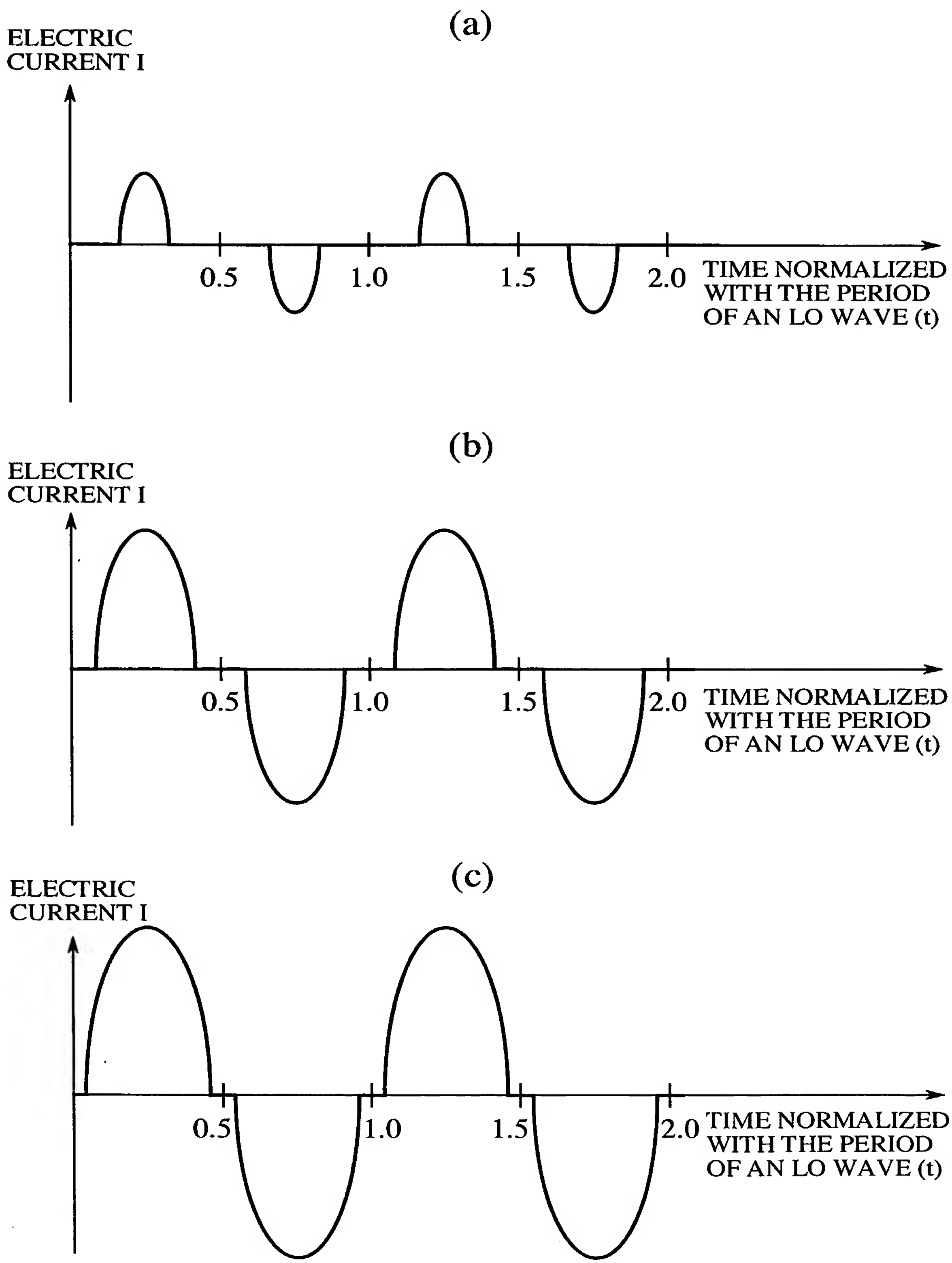

(a)
ELECTRIC
CURRENT I
0.5
1.0
1.5
2.0
TIME NORMALIZED
WITH THE PERIOD
OF AN LO WAVE (t)
(b)
ELECTRIC
CURRENT I
0.5
1.0
1.5
2.0
TIME NORMALIZED
WITH THE PERIOD
OF AN LO WAVE (t)
(c)
ELECTRIC
CURRENT I
0.5
1.0
1.5
2.0
TIME NORMALIZED
WITH THE PERIOD
OF AN LO WAVE (t)

FIG.7

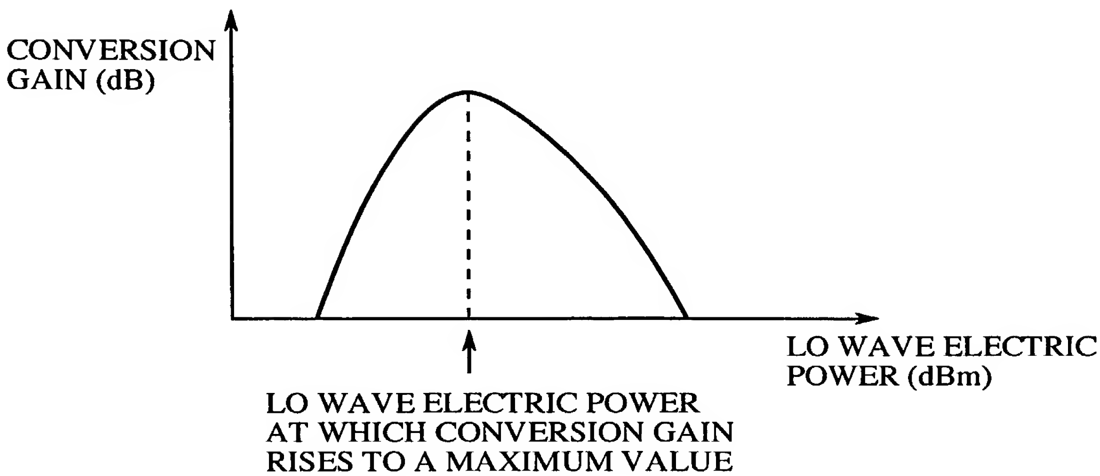

CONVERSION GAIN (dB)
LO WAVE ELECTRIC POWER (dBm)
LO WAVE ELECTRIC POWER AT WHICH CONVERSION GAIN RISES TO A MAXIMUM VALUE

FIG.8

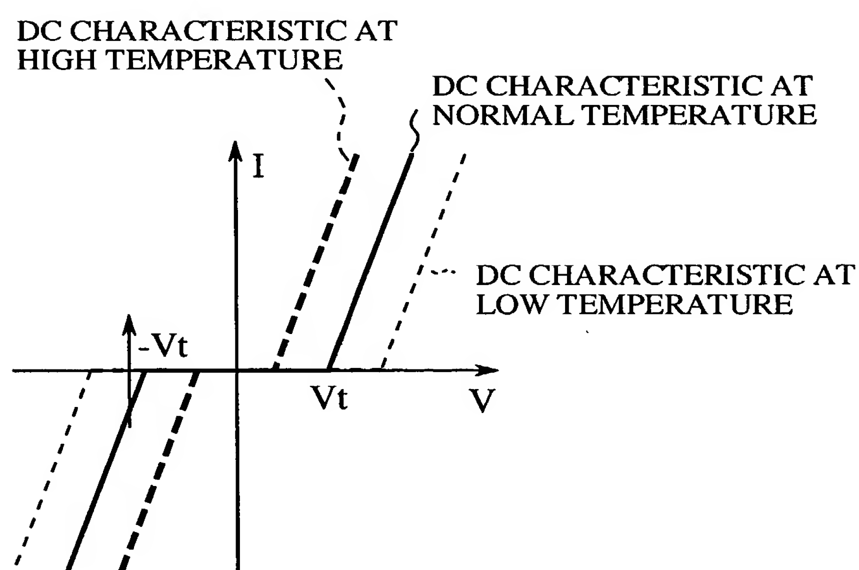

DC CHARACTERISTIC AT HIGH TEMPERATURE
DC CHARACTERISTIC AT NORMAL TEMPERATURE
I
DC CHARACTERISTIC AT LOW TEMPERATURE
-Vt
Vt
V

FIG.9

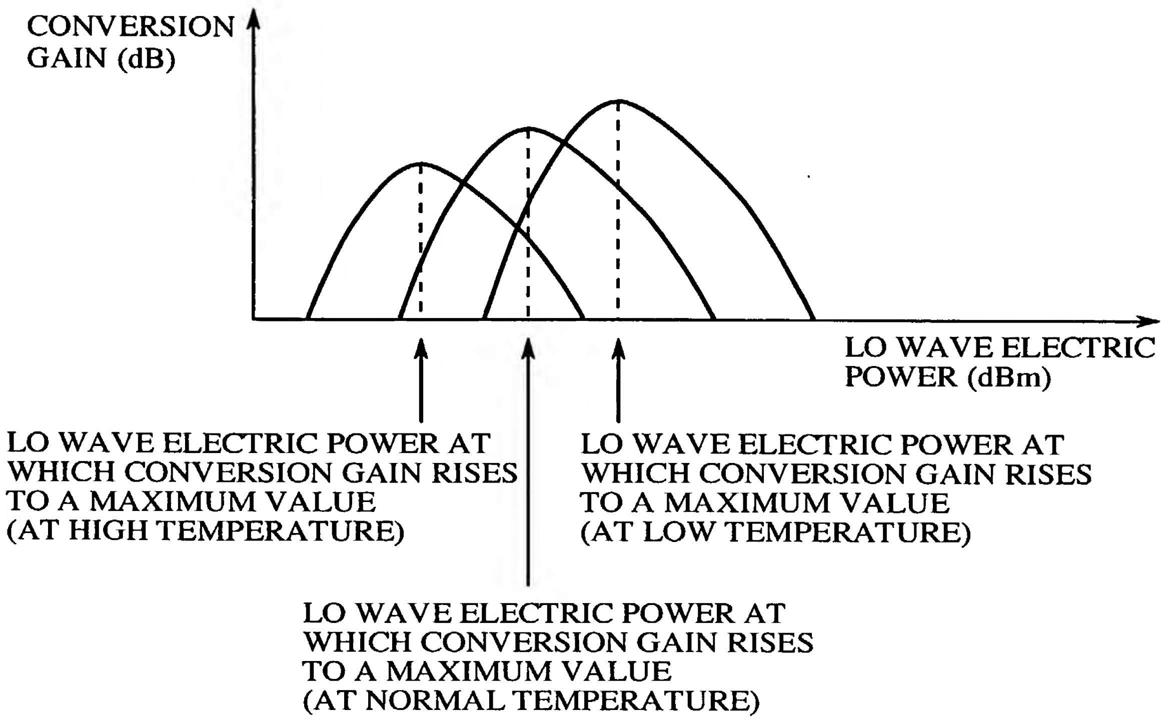

CONVERSION GAIN (dB)
LO WAVE ELECTRIC POWER (dBm)
LO WAVE ELECTRIC POWER AT WHICH CONVERSION GAIN RISES TO A MAXIMUM VALUE (AT HIGH TEMPERATURE)
LO WAVE ELECTRIC POWER AT WHICH CONVERSION GAIN RISES TO A MAXIMUM VALUE (AT LOW TEMPERATURE)
LO WAVE ELECTRIC POWER AT WHICH CONVERSION GAIN RISES TO A MAXIMUM VALUE (AT NORMAL TEMPERATURE)

FIG.10

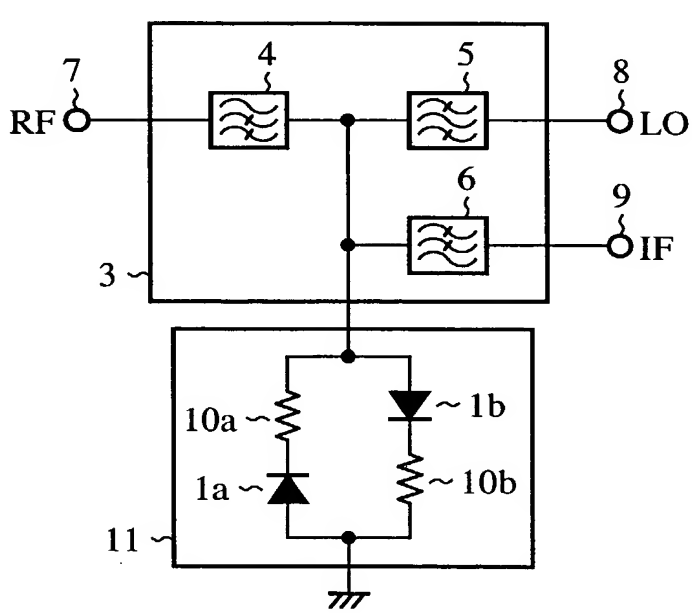

7
RF
4
5
8
LO
6
9
IF
3
10a
1b
1a
10b
11

FIG.11

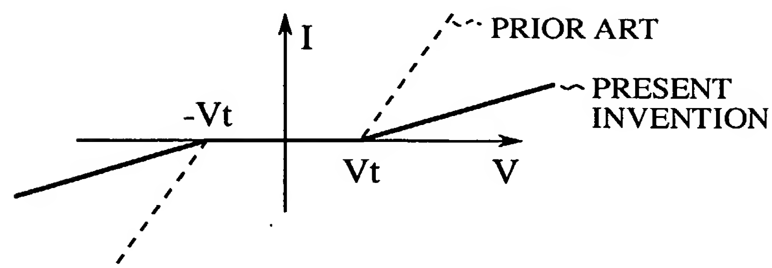


FIG.12

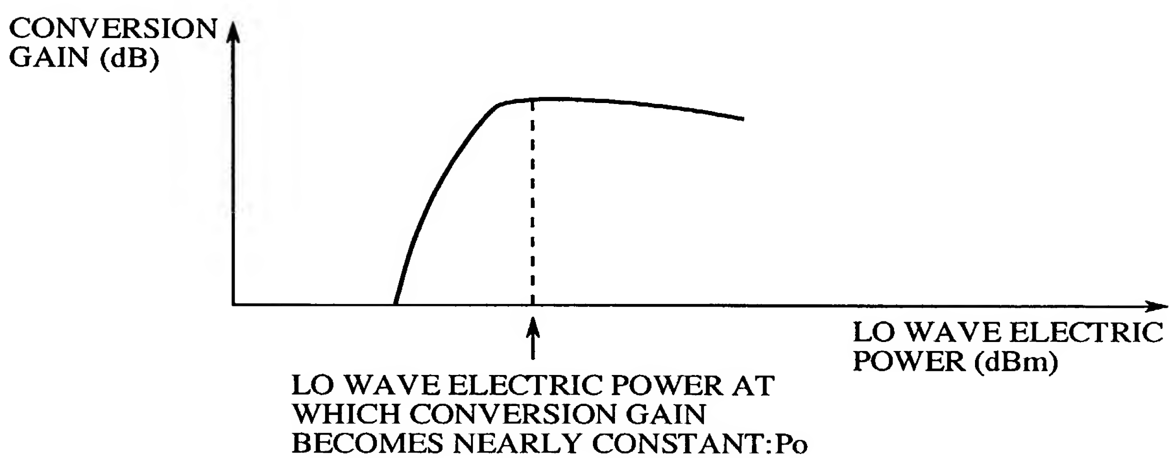


FIG.13

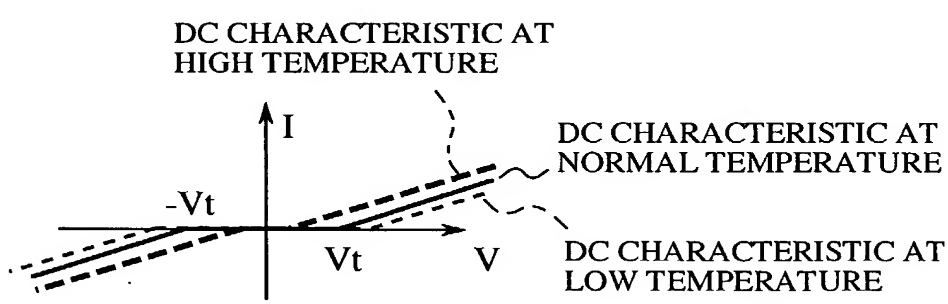


FIG.14

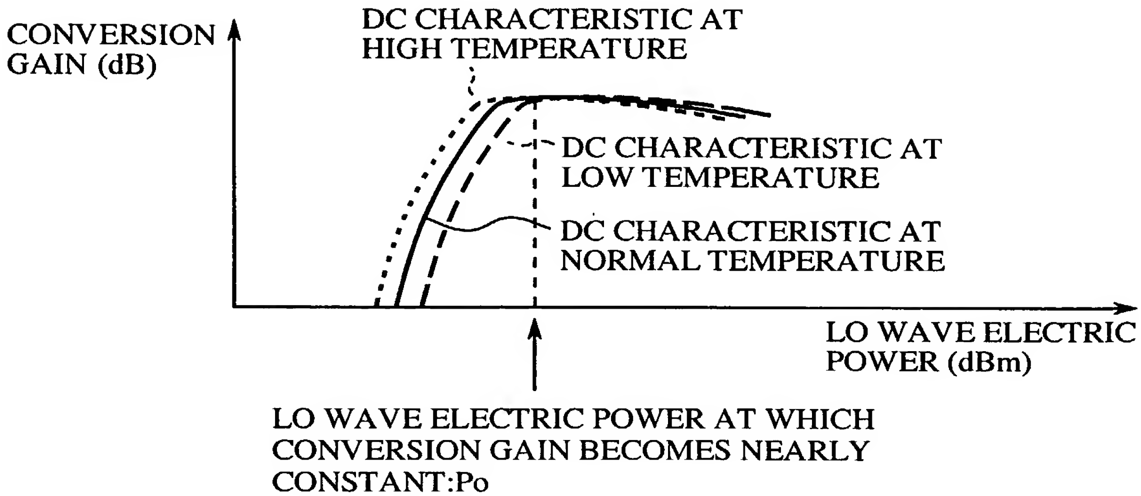

CONVERSION GAIN (dB)
DC CHARACTERISTIC AT HIGH TEMPERATURE
DC CHARACTERISTIC AT LOW TEMPERATURE
DC CHARACTERISTIC AT NORMAL TEMPERATURE
LO WAVE ELECTRIC POWER (dBm)
LO WAVE ELECTRIC POWER AT WHICH CONVERSION GAIN BECOMES NEARLY CONSTANT:Po

FIG.15

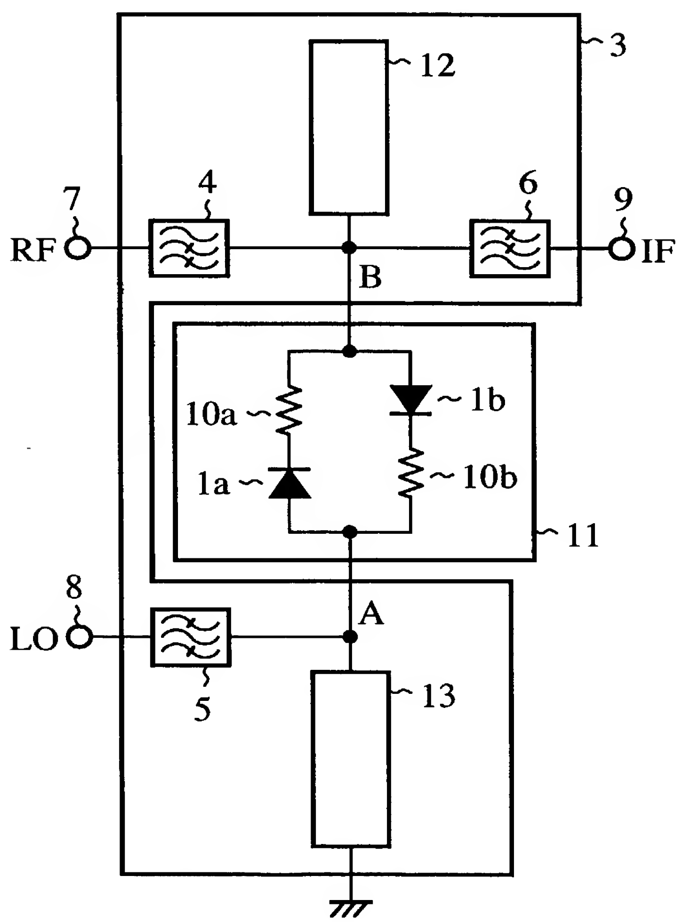

3
12
7
4
6
9
RF
IF
B
10a
1b
1a
10b
11
8
A
LO
5
13

FIG.16

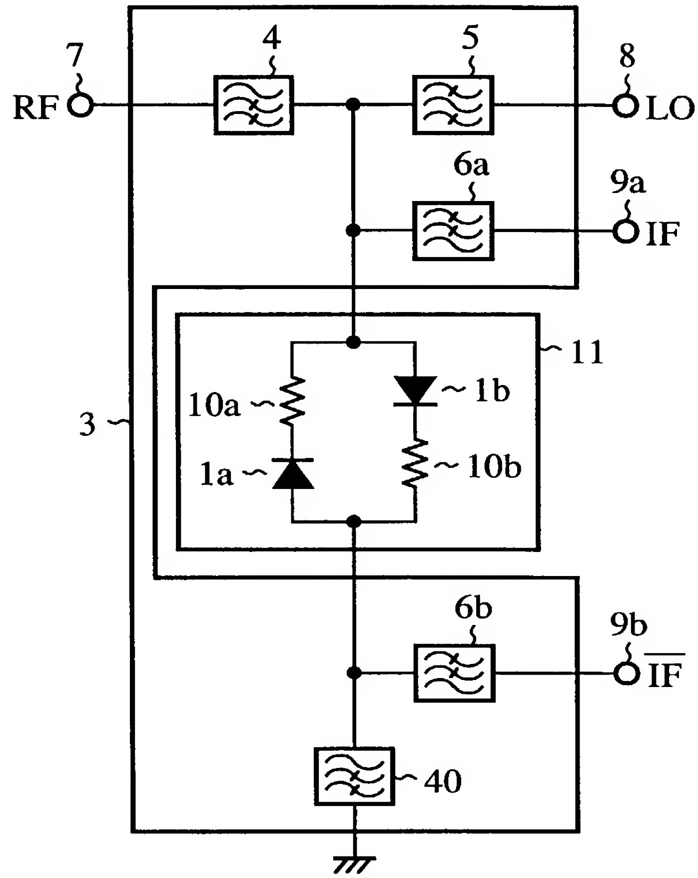

7
RF
4
5
8
LO
6a
9a
IF
11
10a
1b
3
1a
10b
6b
9b
$\overline{\text{IF}}$
40

FIG.17

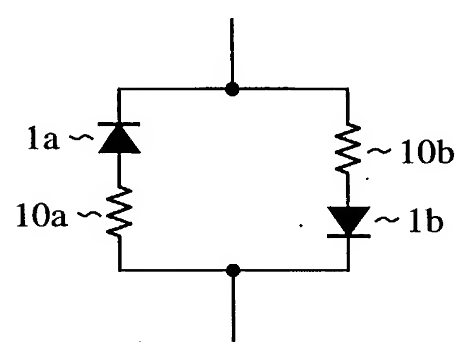

1a
10b
10a
1b

FIG.18

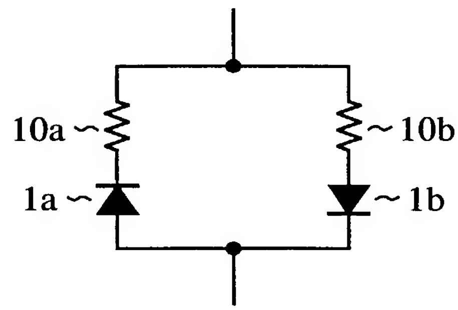


FIG.19

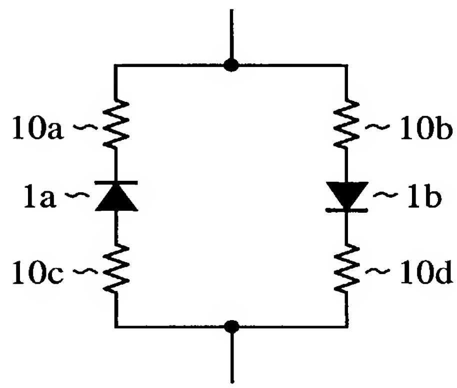


FIG.20

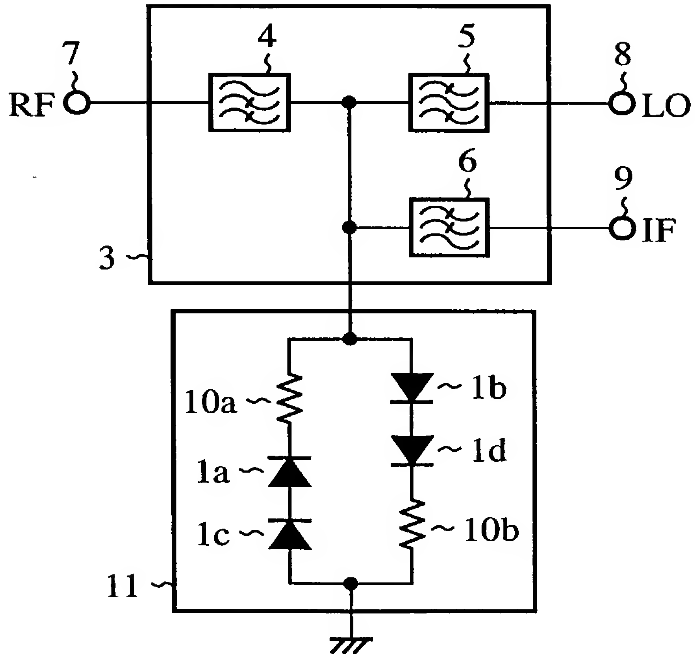


FIG.21

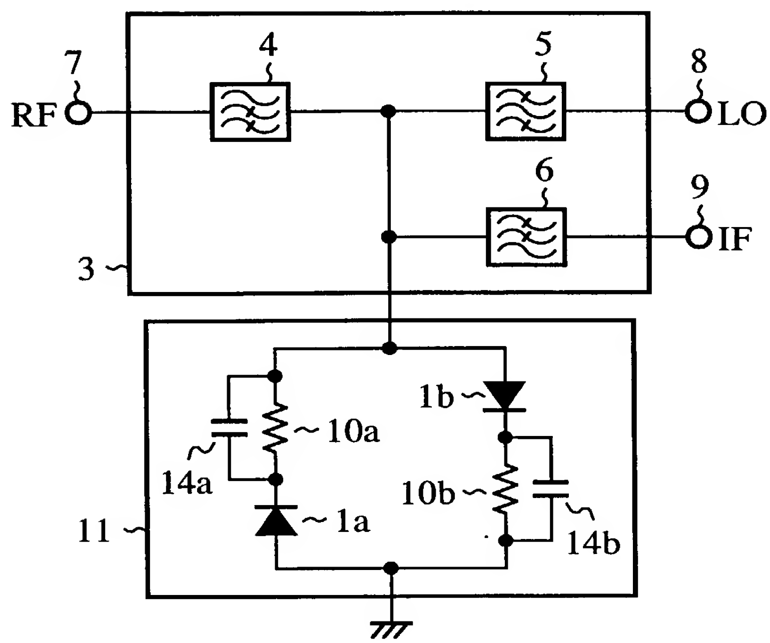

7
RF
4
5
8
LO
6
9
IF
3
1b
10a
14a
10b
1a
11
14b

FIG.22

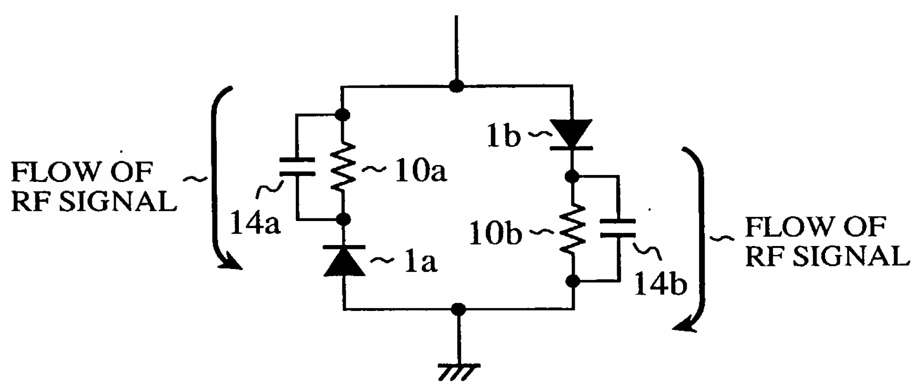

FLOW OF
RF SIGNAL
1b
10a
14a
10b
1a
14b
FLOW OF
RF SIGNAL

FIG.23

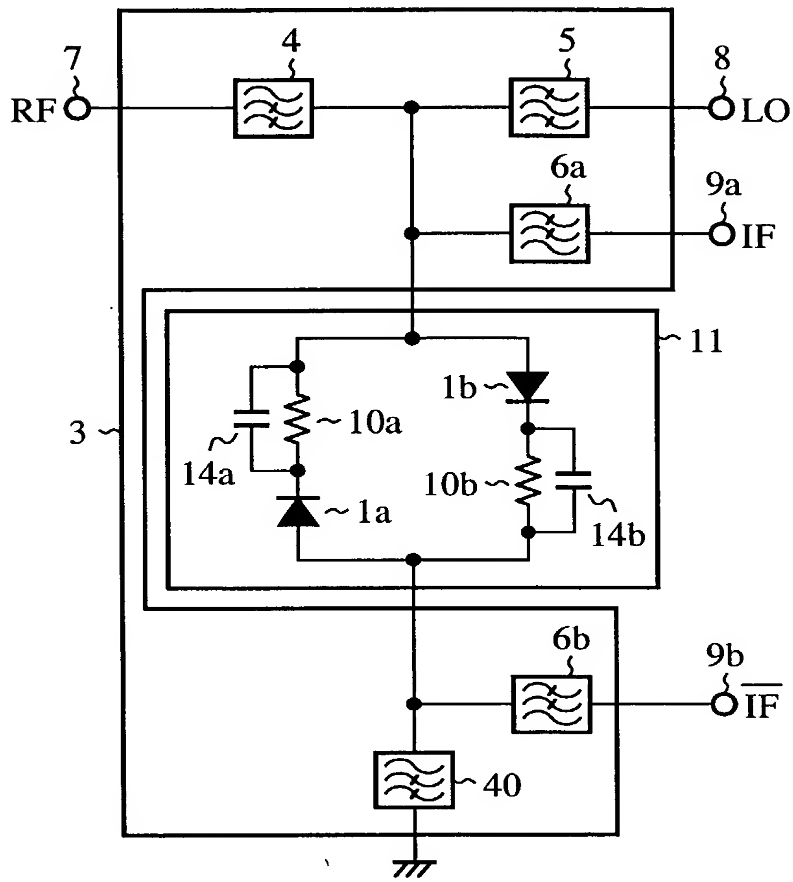

7
RF
4
5
8
LO
6a
9a
IF
11
1b
10a
3
14a
10b
1a
14b
6b
9b
IF
40

FIG.24

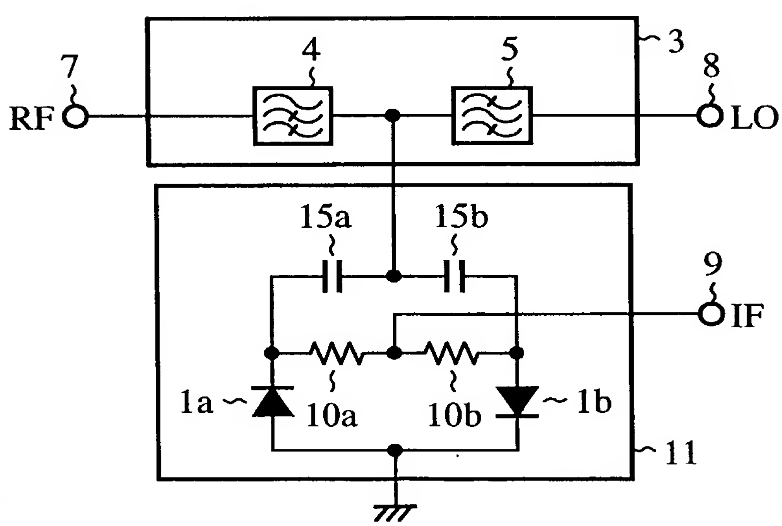

7
RF
4
5
3
8
LO
15a
15b
9
IF
1a
10a
10b
1b
11

FIG.25

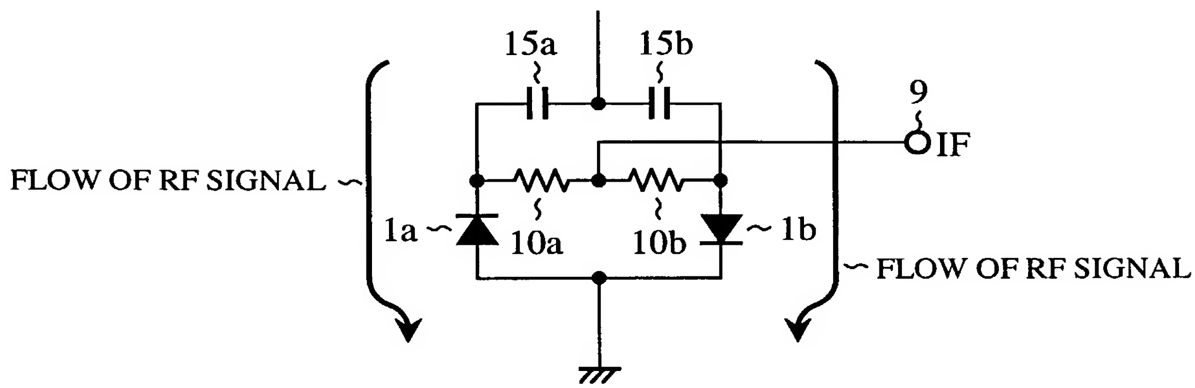
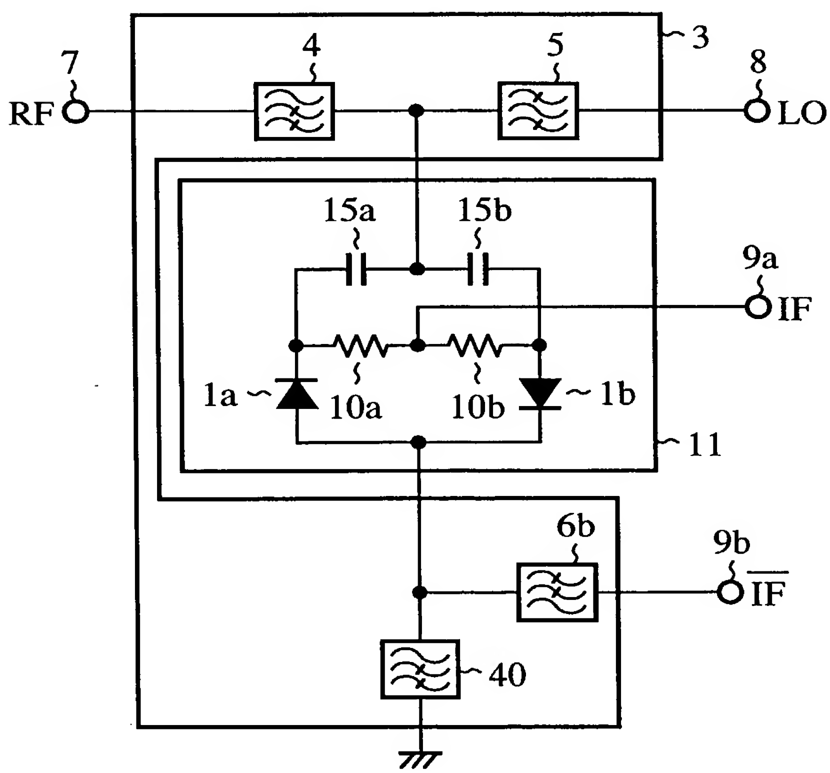

15a
15b
9
IF
FLOW OF RF SIGNAL
1a
10a
10b
1b
FLOW OF RF SIGNAL

FIG.26


4
5
3
7
RF
8
LO
15a
15b
9a
IF
1a
10a
10b
1b
11
6b
9b
IF
40

10069962

FIG.27

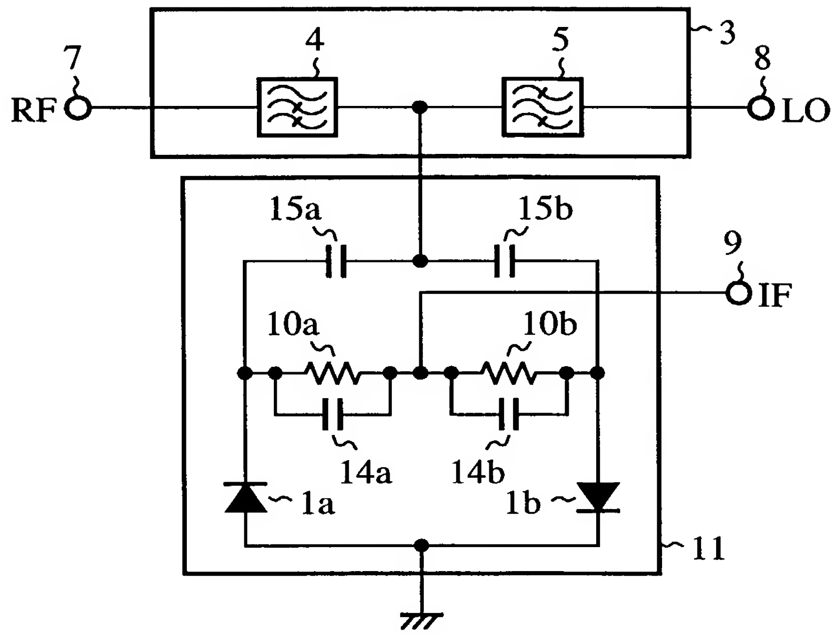


FIG.28

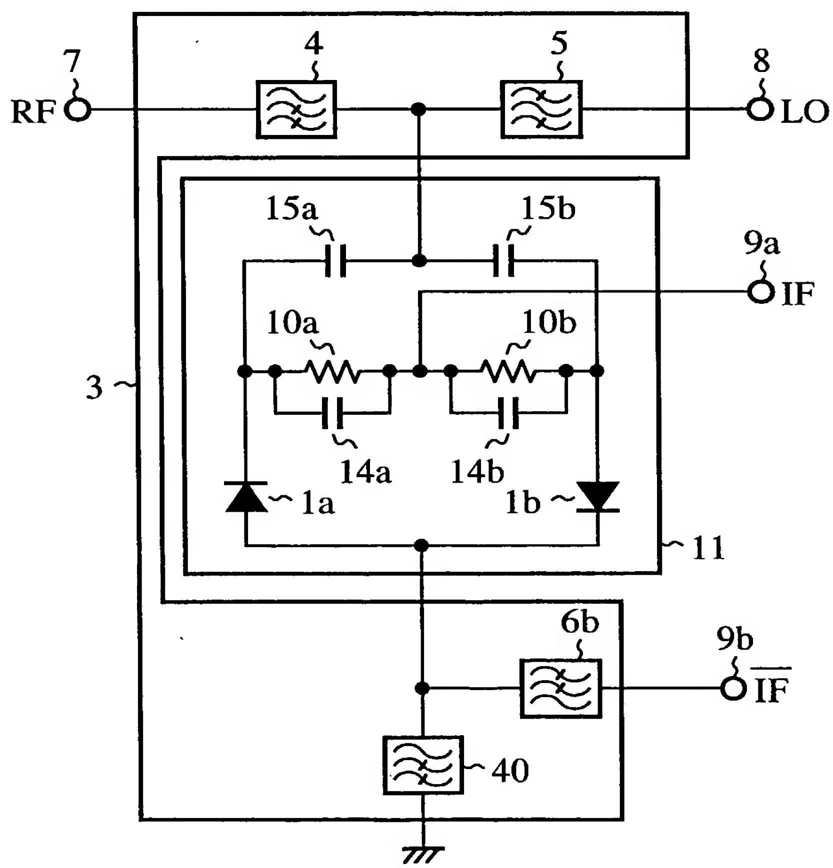


FIG.29

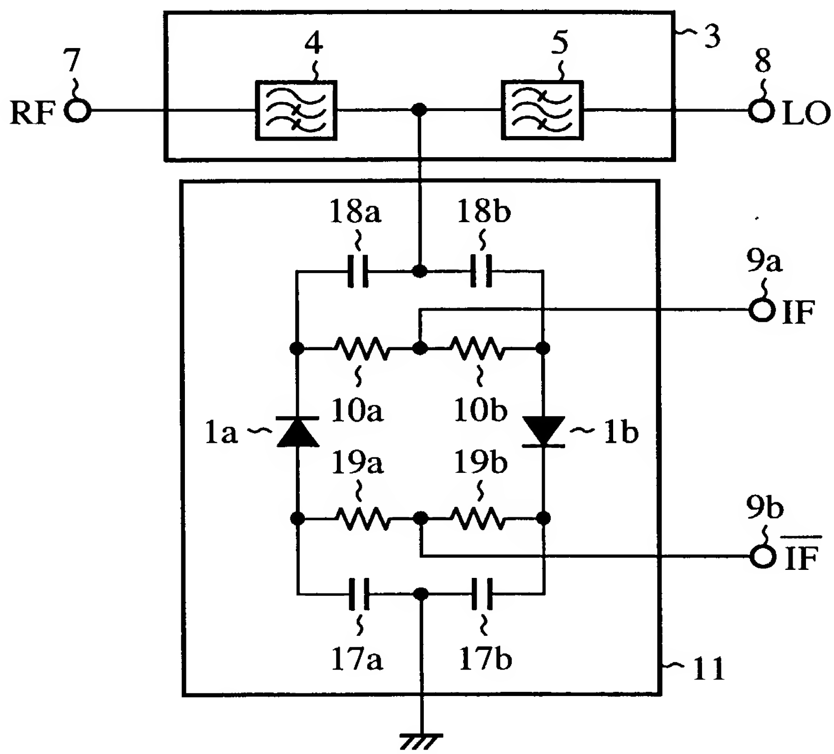
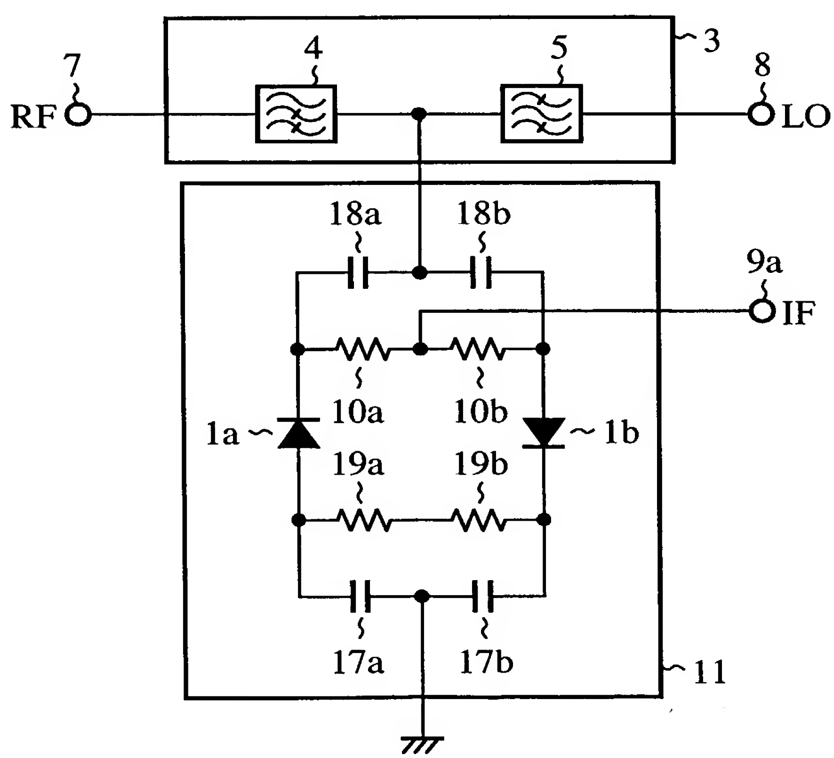

7
RF
4
5
3
8
LO
18a
18b
9a
IF
10a
10b
1a
1b
19a
19b
9b
IF
17a
17b
11

FIG.30


7
RF
4
5
3
8
LO
18a
18b
9a
IF
10a
10b
1a
1b
19a
19b
17a
17b
11

10069962 10/069962

FIG.31

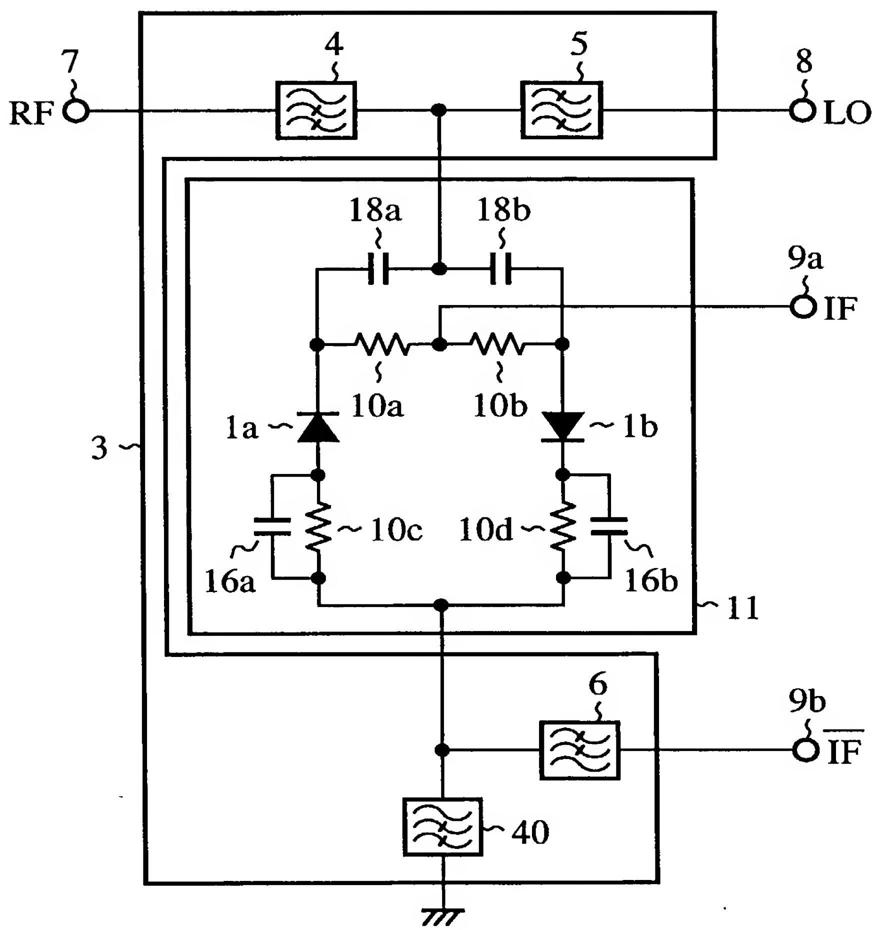


FIG.32

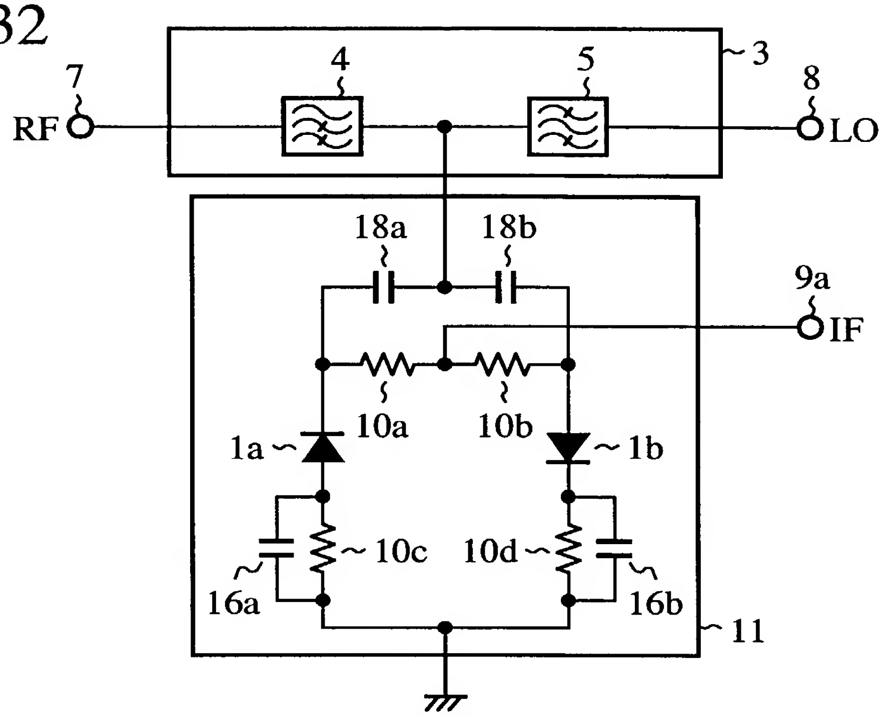

3
4
5
7
RF
8
LO
18a
18b
9a
IF
10a
10b
1a
1b
10c
10d
16a
16b
11

FIG.33

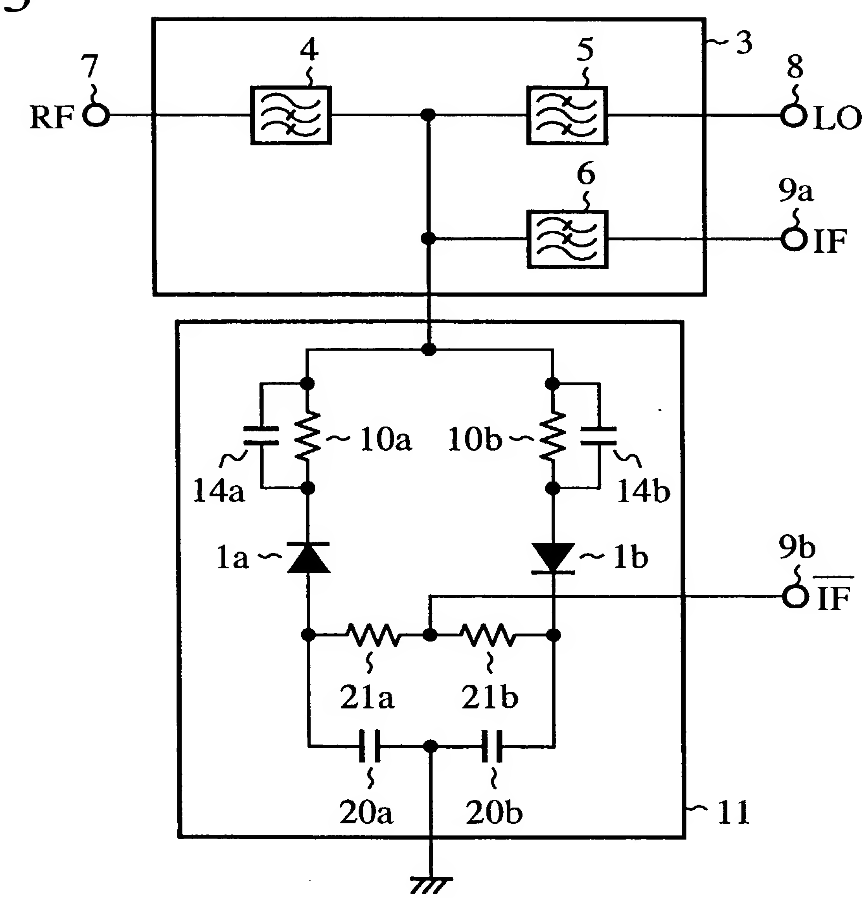
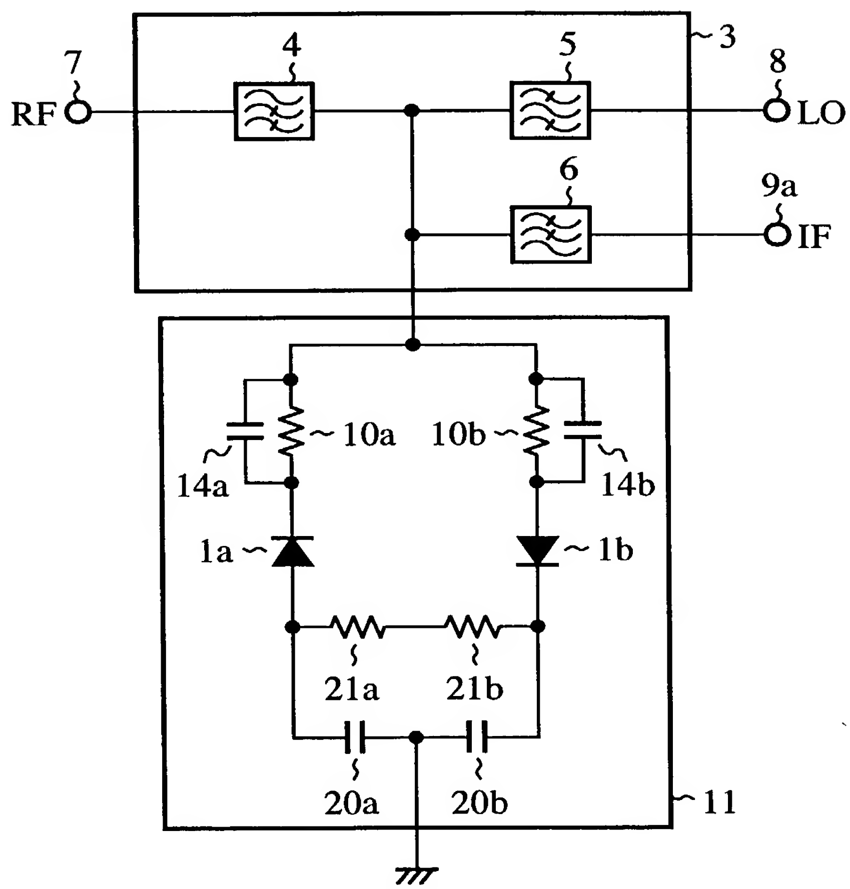

3
4
5
7
RF
8
LO
6
9a
IF
10a
10b
14a
14b
1a
1b
9b
$\overline{\text{IF}}$
21a
21b
20a
20b
11

FIG.34



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

"EVEN HARMONIC MIXER"

上記発明の明細書は、

☐ 本書に添付されています。

☐ ____月____日に提出され、米国出願番号または特許協定条約国際出願番号を____________とし、(該当する場合) ____________に訂正されました。

the specification of which

☐ is attached hereto.

☒ was filed on 10/July/2000 as United States Application Number or PCT International Application Number PCT/JP00/04602 and was amended on ____________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条（a）-（d）項又は365条（b）項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365（a）項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Claimed 優先権主張 ☐ Yes はい	☐ No いいえ
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐ Yes はい	☐ No いいえ

私は、第35編米国法典119条（e）項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条（c）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) （現況：特許許可済、係属中、放棄済）
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) （現況：特許許可済、係属中、放棄済）

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
（日本語宣言書）

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
（弁護士、または代理人の指名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

022850

書類送付先

Send Correspondence to:

022850

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)
(703) 413-3000

単独発明者または第一の共同発明者の氏名 1-00	Full name of sole or first joint inventor Mitsuhiro SHIMOZAWA
発明者の署名 日付	Inventor's signature Date Mitsuhiro Shimozawa Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o MITSUBISHI DENKI KABUSHIKI KAISHA, 2-3, Marunouchi 2-chome,
	Chiyoda-ku, Tokyo 100-8310 Japan
第二の共同発明者の氏名 2-00	Full name of second joint inventor, if any Yoji ISOTA
第二の共同発明者の署名 日付	Second joint Inventor's signature Date Yoji Isota Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o MITSUBISHI DENKI KABUSHIKI KAISHA, 2-3, Marunouchi 2-chome,
	Chiyoda-ku, Tokyo 100-8310 Japan

（第三以降の共同発明者についても同様に記載し、署名すること）

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Declaration
（日本語宣言書）

第三の共同発明者の氏名 3-00	Full name of third joint inventor, if any Tadashi TAKAGI
第三の共同発明者の署名 日付	Third joint Inventor's signature Date Tadashi Takagi Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o MITSUBISHI DENKI KABUSHIKI
	KAISHA, 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan

第四の共同発明者の氏名 4-00	Full name of fourth joint inventor, if any Noriharu SUEMATSU
第四の共同発明者の署名 日付	Fourth joint Inventor's signature Date Noriharu Suematsu Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o MITSUBISHI DENKI KABUSHIKI
	KAISHA, 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan

第五の共同発明者の氏名 5-00	Full name of fifth joint inventor, if any Eiji TANIGUCHI
第五の共同発明者の署名 日付	Fifth joint Inventor's signature Date Eiji Taniguchi Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o MITSUBISHI DENKI KABUSHIKI
	KAISHA, 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan

第六の共同発明者の氏名 6-00	Full name of sixth joint inventor, if any Kenichi MAEDA
第六の共同発明者の署名 日付	Sixth joint Inventor's signature Date Kenichi Maeda Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o MITSUBISHI DENKI KABUSHIKI
	KAISHA, 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan

（第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)

第七の共同発明者の氏名（該当する場合） 7-00	Full name of seventh joint inventor, if any Kenji ITOH
同第七発明者の署名 日付	Seventh inventor's signature Date Kenji Itoh Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post office address c/o MITSUBISHI DENKI KABUSHIKI KAISHA,
	2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan
第八の共同発明者の氏名（該当する場合） 8-00	Full name of eighth joint inventor, if any Takatoshi KATSURA
同第八発明者の署名 日付	Eighth inventor's signature Date Takatoshi Katsura Feb.20, 2002
住所	Residence Tokyo, Japan JPX
国籍	Citizenship Japanese
郵便の宛先	Post office address c/o MITSUBISHI DENKI KABUSHIKI KAISHA,
	2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan
第九の共同発明者の氏名（該当する場合） 9-00	Full name of ninth inventor, if any Takayuki IKUSHIMA
同第九発明者の署名 日付	Ninth inventor's signature Date Takayuki Ikushima Feb.20, 2002
住所	Residence Tokyo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post office address c/o MITSUBISHI DENKI KABUSHIKI KAISHA,
	2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan
第十の共同発明者の氏名（該当する場合）	Full name of tenth joint inventor, if any
同第十発明者の署名 日付	Tenth inventor's signature Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post office address